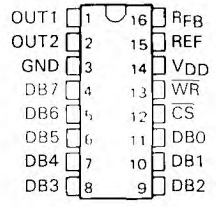
Contents

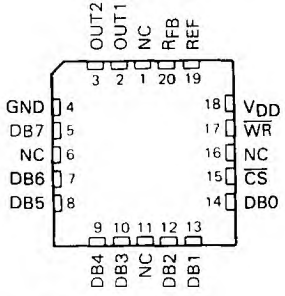
- Advanced LinCMOS™ Silicon-Gate Technology
- Easily Interfaced to Microprocessors
- On-Chip Data Latches
- Monotonicity Over Entire A/D Conversion Range
- Segmented High-Order Bits Ensure Low-Glitch Output
- Designed to be Interchangeable with Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524
- Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	½ LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

N PACKAGE
(TOP VIEW)



AD7524J . . . FN PACKAGE
(TOP VIEW)



NC No internal connection

description

The AD7524 is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The AD7524 is an 8-bit multiplying DAC with input latches and with a load cycle similar to the "write" cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The AD7524 provides accuracy to ½ LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

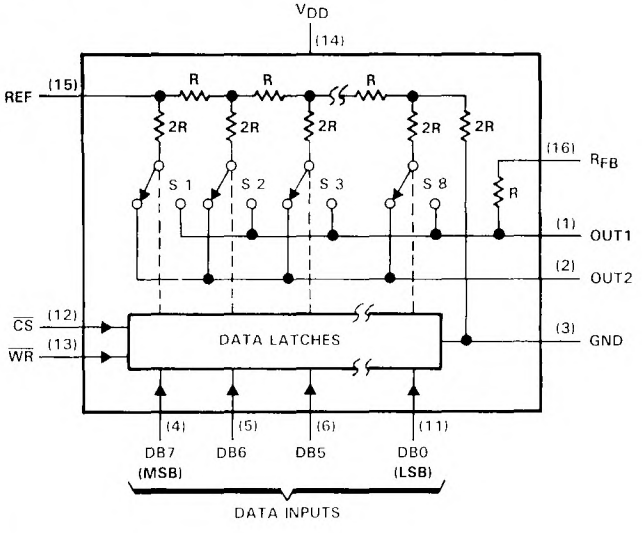
Featuring operation from a 5-V to 15-V single supply, the AD7524 interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the AD7524 an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7524A is characterized for operation from −25°C to 85°C, and the AD7524J is characterized for operation from 0°C to 70°C.

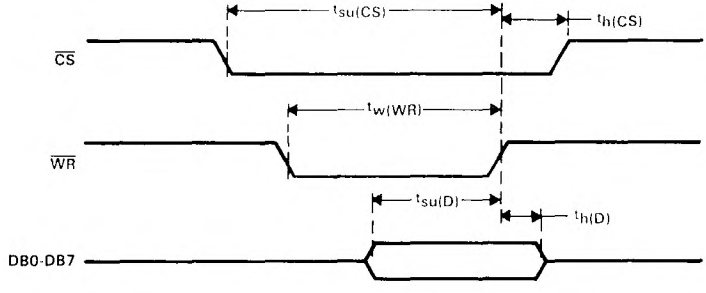
AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING
DEVICE	PACKAGE SUFFIXES	TEMPERATURE RANGE
AD7524A	N	25°C to 85°C
AD7524J	N, FN	0°C to 70°C

functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD}	−0.3 V to 17 V
Voltage between R_{FB} and GND	±25 V
Digital input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Reference voltage, V_{ref}	±25 V
Peak digital input current, I_I	10 μA
Operating free-air temperature range: AD7524A	−25°C to 85°C
AD7524J	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

recommended operating conditions

		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$		40			40			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			0			ns
Data bus input setup time, $t_{su(D)}$		25			25			ns
Data bus input · time, $t_{h(D)}$		10			10			ns
Pulse duration, ∴ ow, $t_{w(WR)}$		40			40			ns
Operating free-air temperature, T_A	AD7524A	−25		85	−25		85	°C
	AD7524J	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$	Full range			10			10	μA
				25°C			1			1	
I_{IL}	Low-level input current		V_I = 0	Full range			−10			−10	μA
				25°C			−1			−1	
I_{lkg}	Output leakage current	OUT1	DB0-DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V, V_{ref} = ±10 V	Full range			±400			±200	nA
				25°C			±50			±50	
		OUT2	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V, V_{ref} = ±10 V	Full range			±400			±200	
				25°C			±50			±50	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max	Full range			2			2	mA
				25°C			1			2	
		Standby	DB0-DB7 at 0 V or V_{DD}	Full range			500			500	μA
				25°C			100			100	
k_{SVS}	Supply voltage sensitivity, $\Delta gain/\Delta V_{DD}$		ΔV_{DD} = 10%	Full range		0.01	0.16		0.005	0.04	%/%
				25°C		0.002	0.08		0.001	0.02	
C_i	Input capacitance, DB0-DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0				5			5	pF
C_o	Output capacitance	OUT1	DB0-DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V				30			30	pF
		OUT2					120			120	
		OUT1	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V				120			120	
		OUT2					30			30	
	Reference input impedance (REF to GND)				5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 15 V		UNIT
			MIN	MAX	MIN	MAX	
Linearity error				±0.2		±0.2	%FSR
Gain error	See Note 1	Full range		±1.4		±0.6	%FSR
		25°C		±1		±0.5	
Settling time (to 1/2 LSB)	See Note 2			100		100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80		80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100 kHz sinewave), $\overline{WR}$ and $\overline{CS}$ at 0, DB0-DB7 at 0	Full range		0.5		0.5	%FSR
		25°C		0.25		0.25	
Temperature coefficient of gain	T_A = 25°C to t_{min} or t_{max}			±0.004		±0.001	%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

PRINCIPLES OF OPERATION

The AD7524 is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the AD7524 D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7524 analog output responds to the data activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The AD7524 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

TEXAS INSTRUMENTS
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PRINCIPLES OF OPERATION

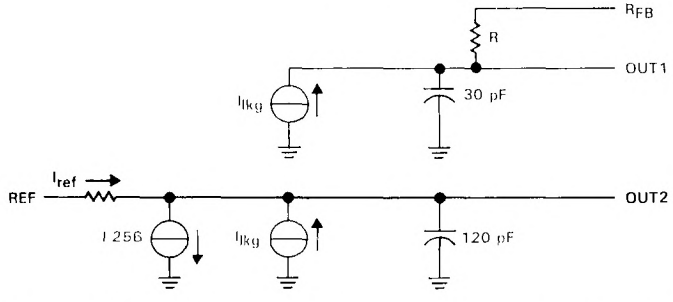

FIGURE 1. AD7524 EQUIVALENT CIRCUIT WITH ALL DIGITAL INPUTS LOW

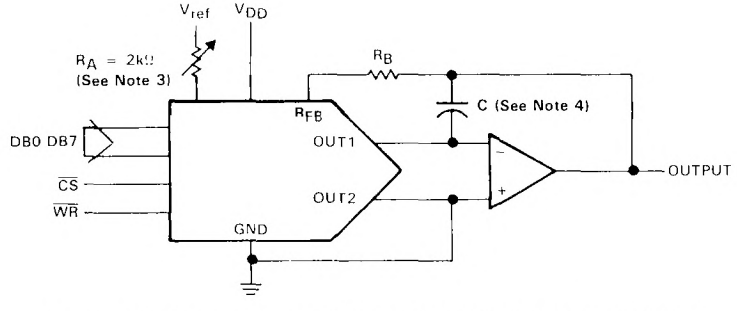

FIGURE 2. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

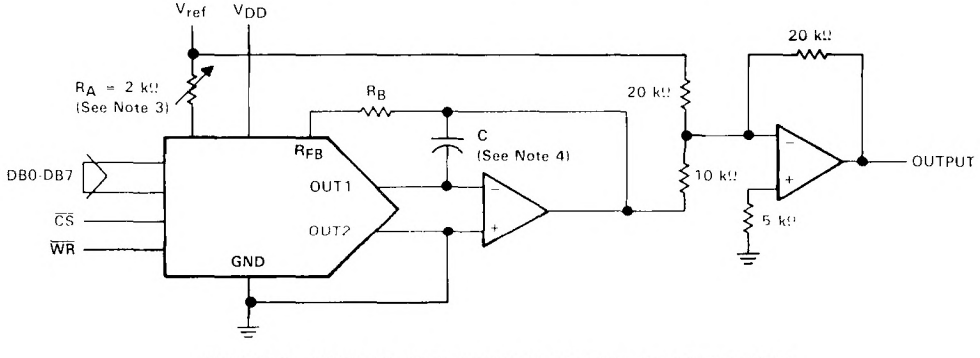

FIGURE 3. BIPOLAR OPERATION (4-QUADRANT OPERATION)

NOTES 3 R_A and R_B used only if gain adjustment is required.
4 C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

PRINCIPLES OF OPERATION

Table 1. Unipolar Binary Code

DIGITAL INPUT (SEE NOTE 5) MSB LSB	ANALOG OUTPUT
11111111	$-V_{ref}$ (255/256)
10000001	$-V_{ref}$ (129/256)
10000000	$-V_{ref}$ (128/256) = $-V_{ref}/2$
01111111	$-V_{ref}$ (127/256)
00000001	$-V_{ref}$ (1/256)
00000000	0

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (SEE NOTE 6) MSB LSB	ANALOG OUTPUT
11111111	V_{ref} (127/128)
10000001	V_{ref} (1/128)
10000000	0
01111111	$-V_{ref}$ (1/128)
00000001	$-V_{ref}$ (127/128)
00000000	$-V_{ref}$

NOTES: 5. LSB = 1/256 (V_{ref}).
6. LSB = 1/128 (V_{ref}).

microprocessor interfaces

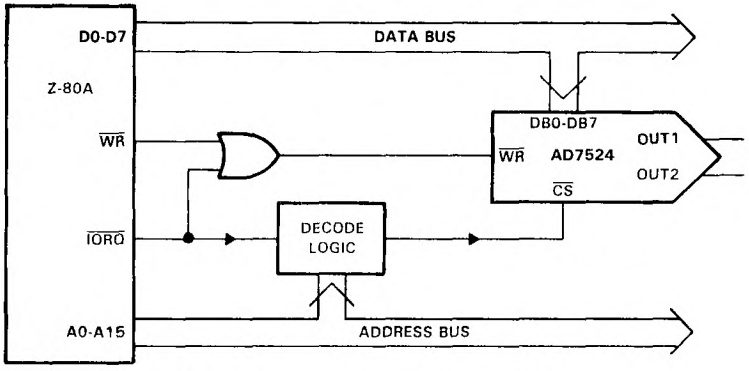

FIGURE 4. AD7524—Z-80A INTERFACE

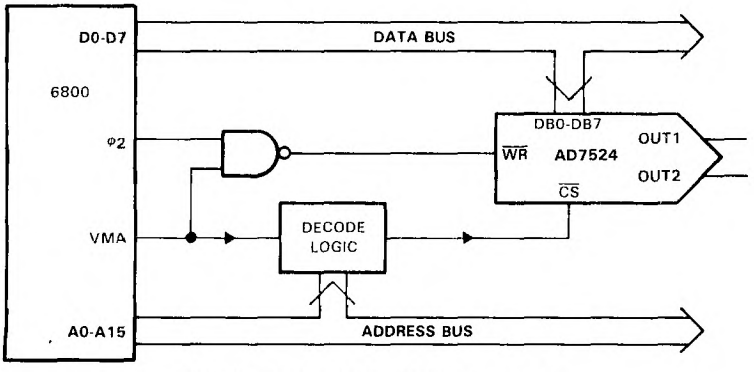

FIGURE 5. AD7524—6800 INTERFACE

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microprocessor interfaces (continued)

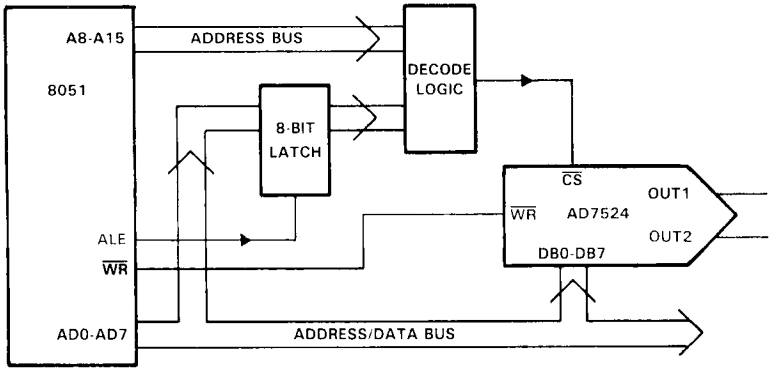
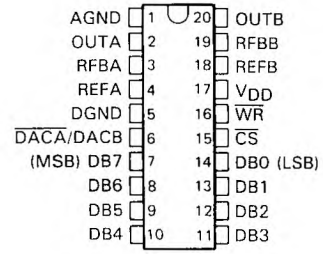


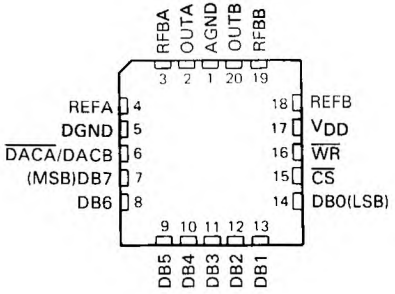
FIGURE 6. AD7524—8051 INTERFACE

- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonic Over the Entire A/D Conversion Range**
- **Designed to be Interchangeable with Analog Devices AD7528 and PMI PM-7528**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at V_{DD} = 5 V	5 mW
Settling Time at V_{DD} = 5 V	100 ns
Propagation Delay at V_{DD} = 5 V	80 ns

description

The AD7528 is a dual 8-bit digital-to-analog converter designed with separate on-chip data latches and featuring excellent DAC-to-DAC matching. Data is transferred to either of the two DAC data latches via a common 8-bit input port. Control input $\overline{DACA}$/DACB determines which DAC is to be loaded. The "load" cycle of the AD7528 is similar to the "write" cycle of a random-access memory, allowing easy interface to most popular microprocessor busses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

The AD7528 operates from a 5-V to 15-V power supply and dissipates less than 15 mW (typical). Excellent 2- or 4-quadrant multiplying makes the AD7528 a sound choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7528B is characterized for operation from −25°C to 85°C. The AD7528K is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING
DEVICE	PACKAGE SUFFIX	TEMPERATURE RANGE
AD7528B	FN, N	25°C to 85°C
AD7528K	FN, N	0°C to 70°C

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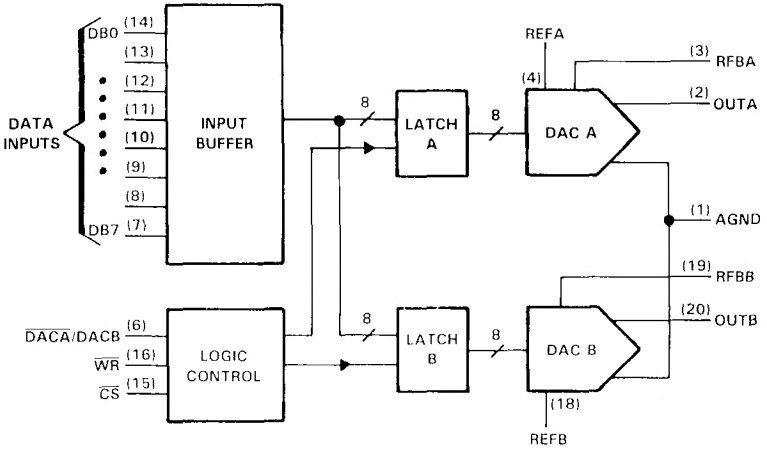
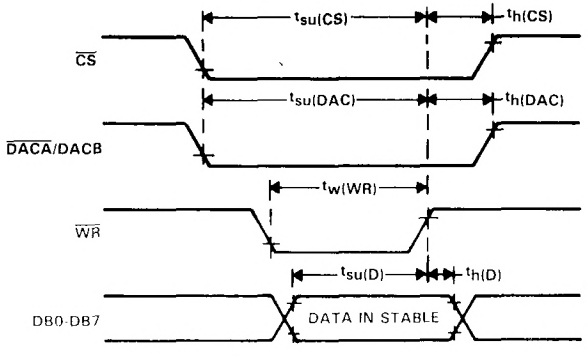
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (to AGND or DGND) . . . . . −0.3 V to 17 V
Voltage between AGND and DGND . . . . . $\pm V_{DD}$
Input voltage, V_I (to DGND) . . . . . −0.3 V to V_{DD} +0.3 V
Reference voltage, V_{refA} or V_{refB} (to AGND) . . . . . ±25 V
Feedback voltage, V_{RFBA} or V_{RFBB} (to AGND) . . . . . ±25 V
Output voltage, V_{OA} or V_{OB} (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 μA
Operating free-air temperature range: AD7528B . . . . . −25°C to 85°C
AD7528K . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

recommended operating conditions

	V_{DD} = 4.75 V to 5.25 V			V_{DD} = 14.5 V to 15.5 V			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Reference voltage, V_{refA} or V_{refB}		±10			10		V
High-level input voltage, V_{IH}	2.4			13.5			V
Low-level input voltage, V_{IL}			0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$	50			50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$	0			0			ns
DAC select setup time, $t_{su(DAC)}$	50			50			ns
DAC select hold time, $t_{h(DAC)}$	10			10			ns
Data bus input setup time $t_{su(D)}$	25			25			ns
Data bus input time $t_{h(D)}$	0			0			ns
Pulse duration, ow, $t_{w(WR)}$	50			50			ns
Operating free-air temperature, T_A AD	−25		85	−25		85	°C
AD	0		70	0		70	

electrical characteristics over recommended operating temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V MIN	V_{DD} = 5 V MAX	V_{DD} = 15 V MIN	V_{DD} = 15 V MAX	UNIT
I_{IH}	High-level input current		$V_I = V_{DD}$	Full Range		10		10	μA
				25°C		1		1	
I_{IL}	Low-level input current		V_I = 0	Full Range		−10		−10	μA
				25°C		−1		−1	
	Reference input impedance (Pin 15 to GND)				8	15	8	15	kΩ
I_{lkg}	Output leakage current	OUTA	DAC data latch loaded with 00000000, V_{refA} = ±10 V	Full Range		±400		±200	nA
				25°C		±50		±50	
		OUTB	DAC data latch loaded with 00000000, V_{refB} = ±10 V	Full Range		±400		±200	
				25°C		±50		±50	
	Input resistance match (REFA to REFB)					±1%		±1%	
	DC supply sensitivity Δgain/ΔV_{DD}		V_{DD} = ±10%	Full Range		0.04		0.02	%/%
				25°C		0.02		0.01	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max			1		1	mA
		Standby	DB0-DB7 at 0 V or V_{DD}	Full Range		0.5		0.5	
				25°C		0.1		0.1	
C_i	Input capacitance	DB0-DB7	V_I = 0 or V_{DD}			10		10	pF
		$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$/DACB				15		15	
C_o	Output capacitance (OUTA, OUTB)		DAC Data latches loaded with 00000000			50		50	pF
			DAC Data latches loaded with 11111111			120		120	

operating characteristics over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error						±1/2			±1/2	LSB
Setting time (to 1/2 LSB)		See Note 1				100			100	ns
Gain error		See Note 2	Full Range			±4			±3	LSB
			25°C			±2			±2	
AC feedthrough	REFA to OUTA	See Note 3	Full Range			−65			−65	dB
	REFB to OUTB		25°C			−70			−70	
Temperature coefficient of gain						0.007			0.00[illegible]	
Propagation delay (from digital input to 90% of final analog [illegible]t current)		See Note 4				80			80	ns
Channel-to-channel isolation	[illegible] to OUTB	See Note 5	25°C		77			77		dB
	REFB to OUTA	See Note 6	25°C		77			77		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C			160			440		nVs
Digital crosstalk glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C			30			60		nVs
Harmonic distortion		V_i = 6 V, f = 1 kHz, T_A = 25°C			−85			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
3. V_{ref} = 20 V peak-to-peak, 100-kHz sine wave; DAC data latches loaded with 0000000.
4. V_{refA} = V_{refB} = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V
5. Both DAC latches loaded with 11111111; V_{refA} = 20 V peak-to-peak, 100-kHz sine wave; V_{refB} = 0.
6. Both DAC latches loaded with 11111111; V_{refB} = 20 V peak-to-peak, 100-kHz sine wave; V_{refA} = 0.

principles of operation

The AD7528 contains two identical 8-bit multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground pin 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_O is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_O is 50 pF to 120 pF maximum. The equivalent output resistance r_O varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

Interfacing the AD7528 to a microprocessor is accomplished via the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7528 analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When e[illegible] the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs is latched until the $\overline{CS}$ and [illegible] signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The digital inputs of the AD7528 provide TTL compatibility when operated from a supply voltage of 5 V. The AD7528 may be operated with any supply voltage in the range from 5 V to 15 V, however, input logic levels are not TTL compatible above 5 V.

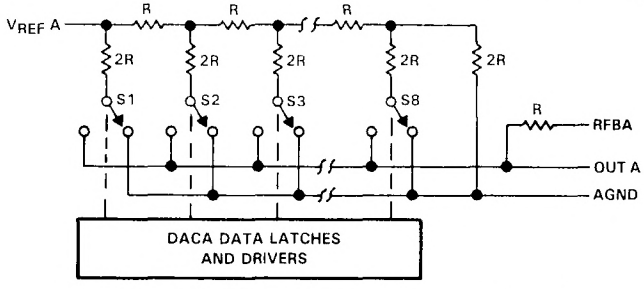


FIGURE 1. SIMPLIFIED FUNCTIONAL CIRCUIT FOR DACA

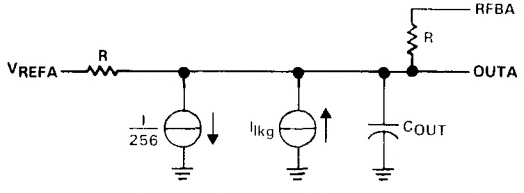


FIGURE 2. AD7528 EQUIVALENT CIRCUIT, DACA LATCH LOADED WITH 11111111.

MODE SELECTION TABLE

$\overline{DACA}$/DACB	$\overline{CS}$	$\overline{WR}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = low level H = high level X = don't care

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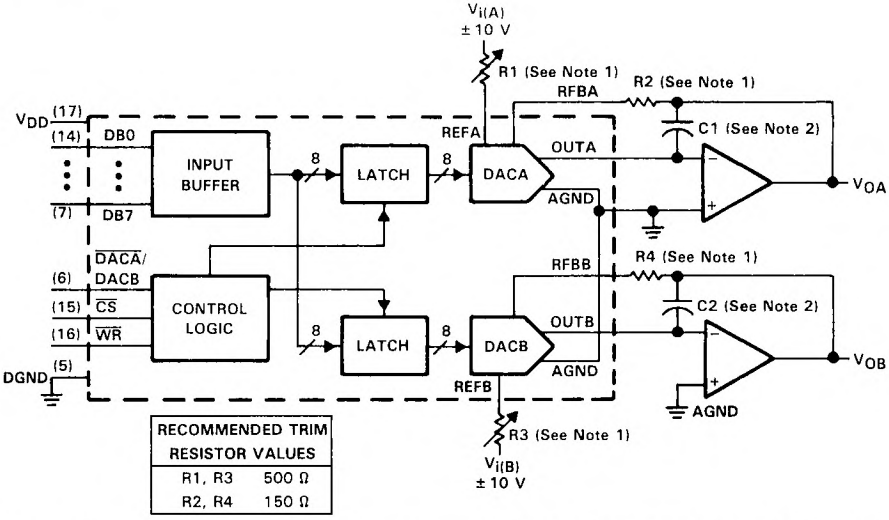
TYPICAL APPLICATION DATA

The AD7528 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

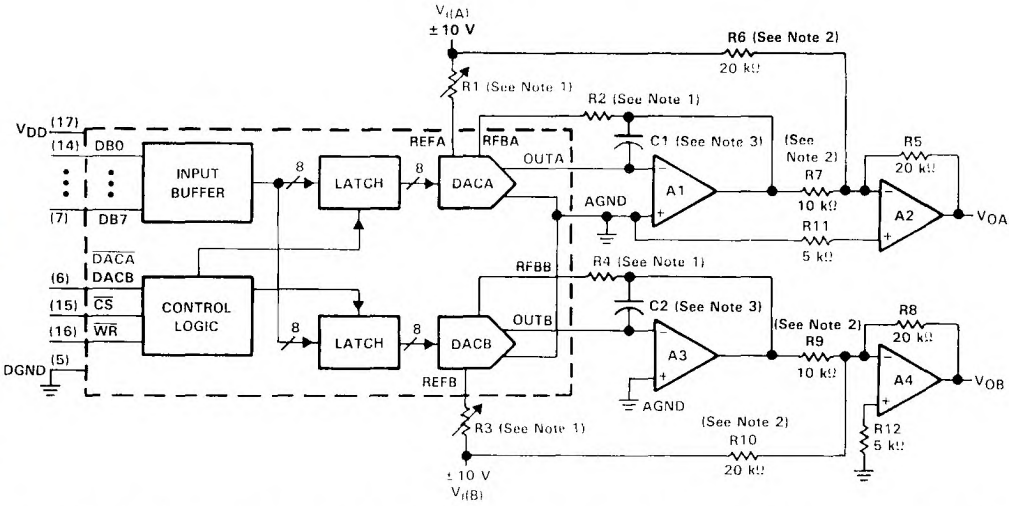


RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
2. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

FIGURE 3. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

TYPICAL APPLICATION DATA



NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
2. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
3. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers.

FIGURE 4. BIPOLAR OPERATION (4-QUADRANT OPERATION)

TABLE 1. UNIPOLAR BINARY CODE

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
11111111	V_I (255/256)
10000001	V_I (129/256)
10000000	V_I (128/256) = $V_I/2$
01111111	V_I (127/256)
00000001	V_I (1/256)
00000000	$-V_I$ (0/256) = 0

† 1 LSB = $(2^{-8})V_I$

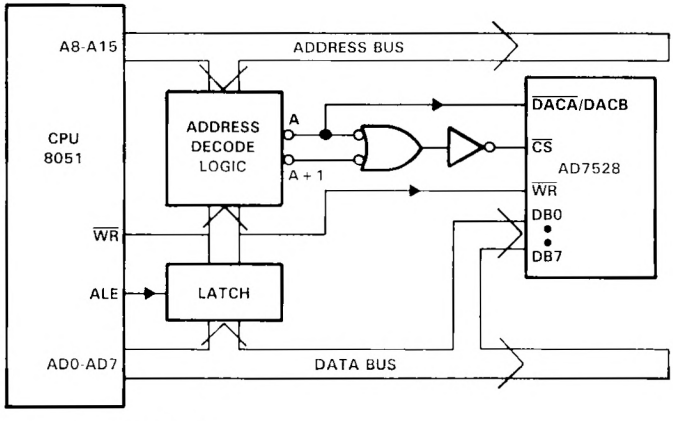
TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
11111111	V_I (127/128)
10000001	V_I (1/128)
10000000	0 V
01111111	V_I (1/128)
00000001	V_I (127/128)
00000000	$-V_I$ (128/128)

‡ 1 LSB = $(2^{-7})V_I$

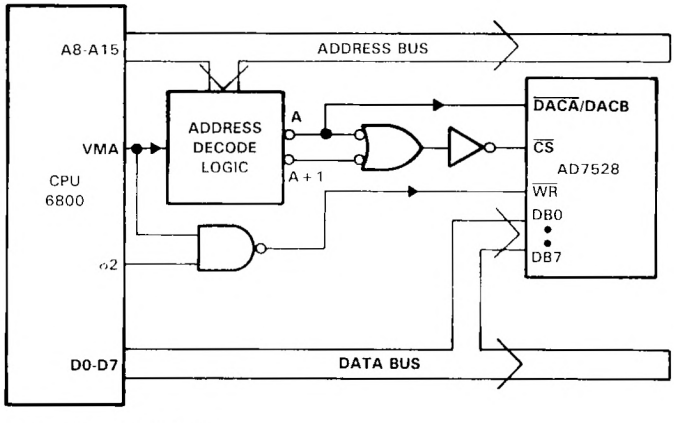
TYPICAL APPLICATION DATA

microprocessor interface information



NOTE: A = decoded address for AD7528 DACA
A + 1 = decoded address for AD7528 DACB

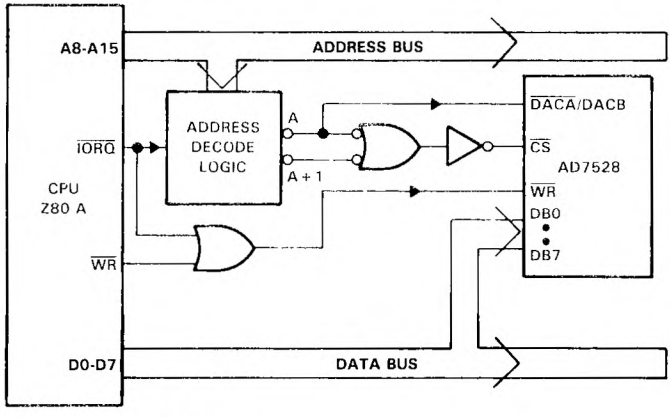
FIGURE 5. AD7528 — INTEL 8051 INTERFACE



NOTE: A = decoded address for AD7528 DACA.
A + 1 = decoded address for AD7528 DACB.

FIGURE 6. AD7528 — 6800 INTERFACE

TYPICAL APPLICATION DATA



NOTE. A = decoded address for AD7528 DACA.
A + 1 = decoded address for AD7528 DACB.

FIGURE 7. AD7528 TO Z-80A INTERFACE

programmable window detector

The programmable window comparator shown in Figure 8 will determine if voltage applied to the DAC feedback resistors are within the limits programmed into the AD7528 data latches. Input signal range depends on the reference and polarity, that is, the test input range is 0 to $-V_{ref}$. The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output high.

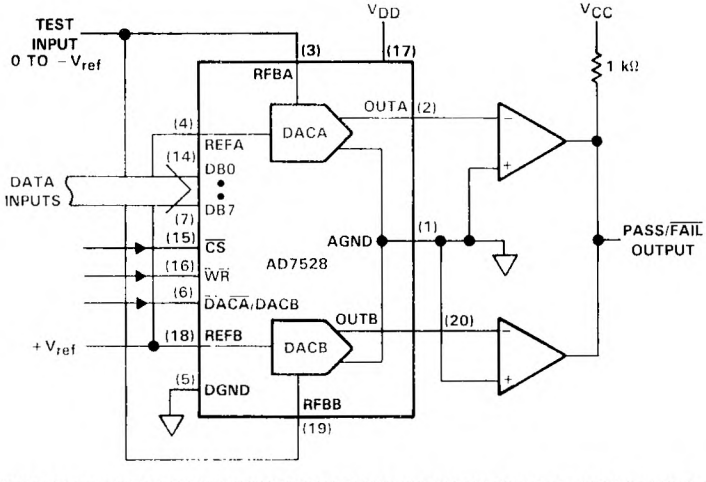


FIGURE 8. DIGITALLY PROGRAMMABLE WINDOW COMPARATOR (UPPER- AND LOWER-LIMIT TESTER)

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TYPICAL APPLICATION DATA

digitally controlled signal attenuator

Figure 9 shows the AD7528 configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5 dB range.

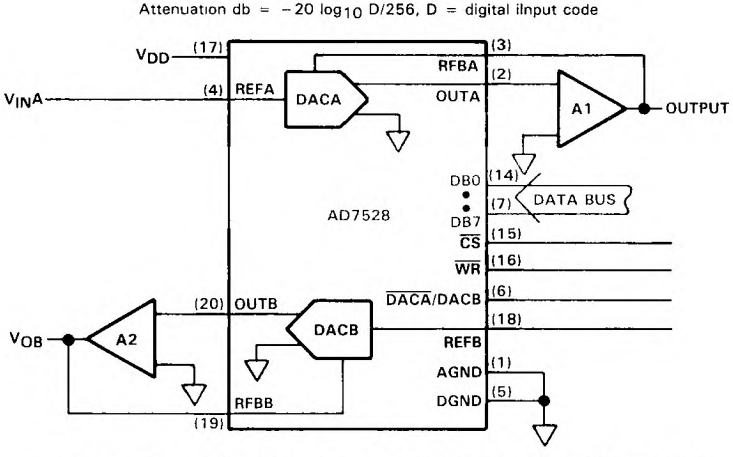


FIGURE 9. DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR

TABLE 3. ATTENUATION vs DACA, DACB CODE

ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL	ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	.	9.0	01011011	91
1.5	11010111		9.5	01010110	86
2.0	11001011		10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5			12.5	00111101	61
5.0			13.0	00111001	57
5.5		136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	011	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43

TYPICAL APPLICATION DATA

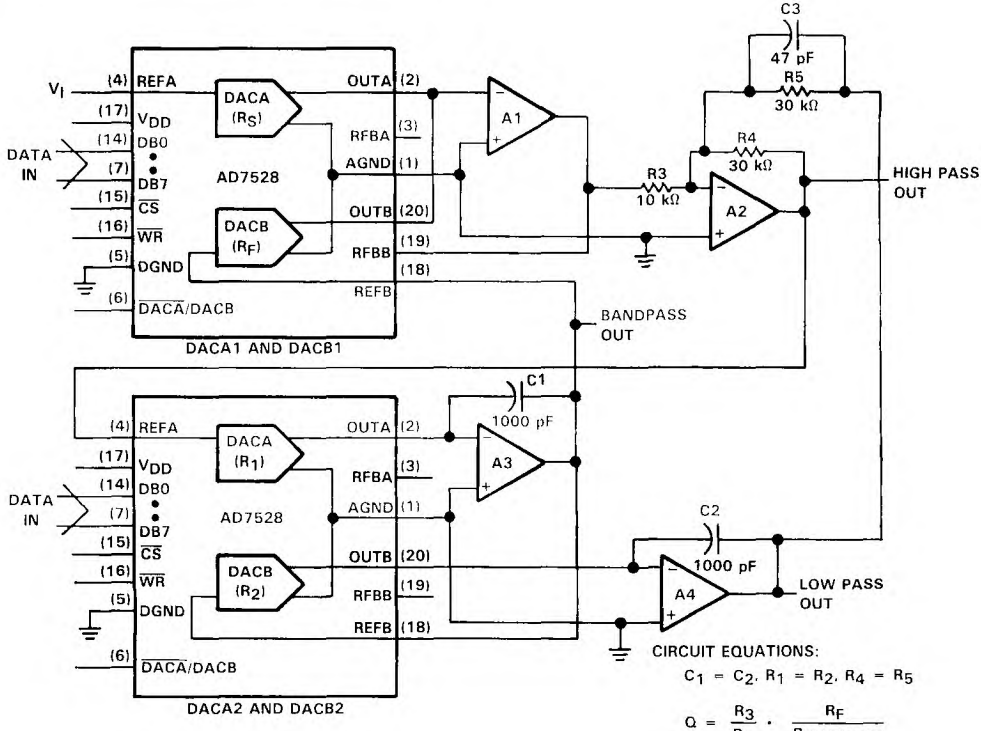
programmable state-variable filter

This programmable state-variable or universal filter configuration provides low-pass, high-pass, and band-pass outputs, and is suitable for applications in which microprocessor control of filter parameters is required.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the AD7528, this is easily achieved.

$$f_C = \frac{1}{2\pi\, R1\, C1}$$

The programmable range for the cutoff or center frequency is 0 to 15 kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.



NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.

B. C3 compensates for the op-amp gain-bandwidth limitations.

C. DAC equivalent resistance equals $\frac{256 \times \text{(DAC ladder resistance)}}{\text{DAC digital code}}$

FIGURE 10. DIGITALLY CONTROLLED STATE-VARIABLE FILTER

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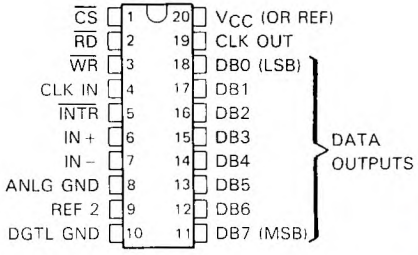
D2754, NOVEMBER 1983 REVISED SEPTEMBER 1986

- 8-Bit Resolution
- Ratiometric Conversion
- 100-μs Conversion Time
- 135-ns Access Time
- Guaranteed Monotonicity
- High Reference Ladder Impedance . . . 8 kΩ Typical
- No Zero Adjust Requirement
- On-Chip Clock Generator
- Single 5-V Power Supply
- Operates with Microprocessor or as Stand-Alone
- Designed to be Interchangeable with National Semiconductor and Signetics ADC0803 and ADC0805

N PACKAGE
(TOP VIEW)



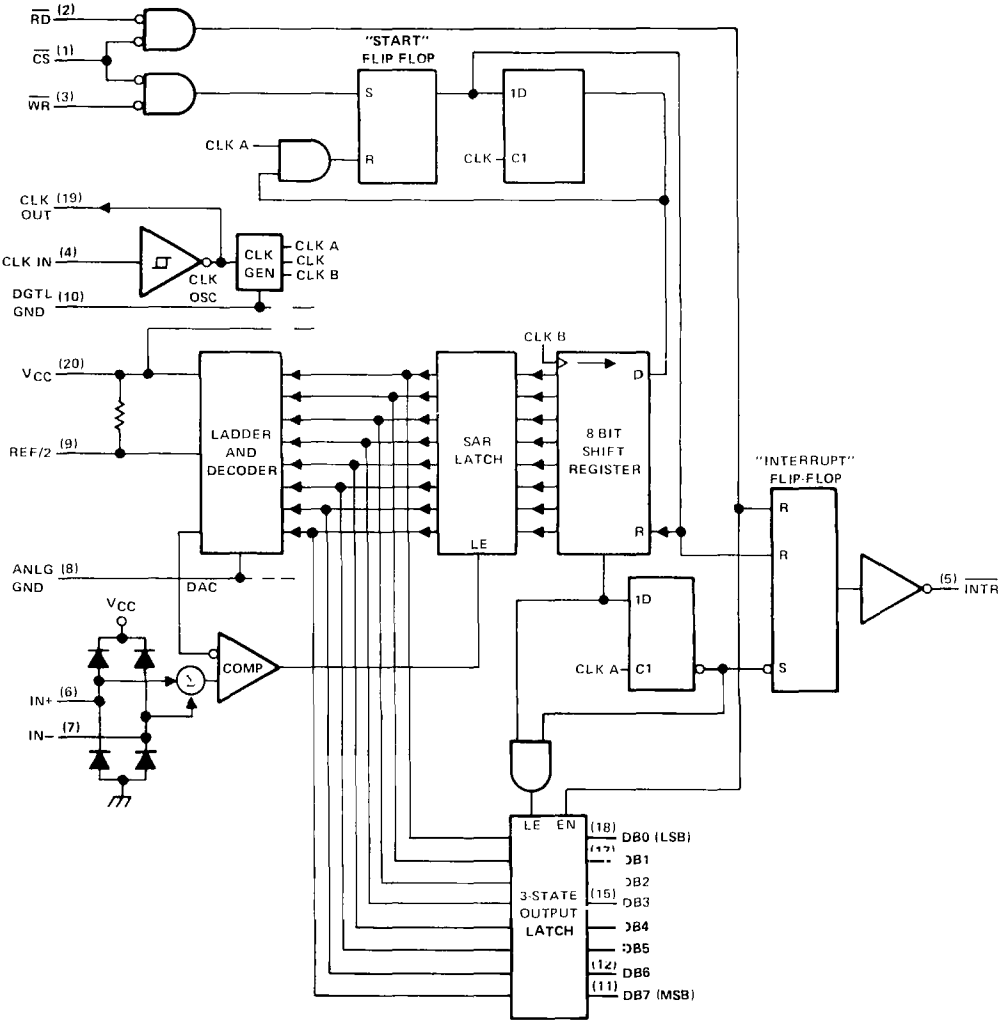
description

The ADC0803 and ADC0805 are CMOS 8-bit, successive-approximation, analog-to-digital converters that use a modified potentiometric (256R) ladder. These devices are designed to operate from common microprocessor control buses with the three-state output latches driving the data bus. The devices can be made to appear to the microprocessor as a memory location or an I/O port. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

A differential analog voltage input allows increased common-mode rejection and offset of the zero-input analog voltage value. Although a reference input (REF/2) is available to allow 8-bit conversion over smaller analog voltage spans or to make use of an external reference, ratiometric conversion is possible with the REF/2 input open. Without an external reference, the conversion takes place over a span from V_{CC} to analog ground (ANLG GND). The devices can operate with an external clock signal or, with an additional resistor and capacitor, using an on-chip clock generator.

The ADC0803I and ADC0805I are characterized for operation from −40°C to 85°C. The ADC0803C and ADC0805C are characterized for operation from 0°C to 70°C.

functional block diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ . . . . . −0.3 V to 18 V
Other inputs . . . . . −0.3 V to V_{CC} +0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} +0.3 V
Operating free-air temperature range: ADC080_I . . . . . −40°C to 85°C
ADC080_C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to digital ground (DGTL GND) with DGTL GND and ANLG GND connected together unless otherwise noted.

recommended operating conditions

		MIN		MAX	UNIT
Supply voltage, V_{CC}		4.5		6.3	V
Analog input voltage (see Note 2)		−0.05		V_{CC}+0.05	V
Voltage at REF/2 (see Note 3), $V_{REF/2}$		0.25	2.5		V
High-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$, V_{IH}		2		15	V
Low-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$, V_{IL}				0.8	V
Analog ground voltage (see Note 4)		−0.05	0	1	V
Clock input frequency (see Note 5), f_{clock}		100	640	1460	kHz
Duty cycle for f_{clock} above 640 kHz (see Note 5)		40%		60%	
Pulse duration, clock input (high or low) for f_{clock} below 640 kHz, $t_{w(CLK)}$		275	781		ns
Pulse duration, $\overline{WR}$ input low, $t_{w(WR)}$		100			ns
Operating free-air temperature, T_A	ADC080_I	−40		85	°C
	ADC080_C	0		70	

NOTES: 2. When the differential input voltage ($V_{I+} - V_{I-}$) is less than or equal to 0 V, the output code is 0000 0000.
3. The internal reference voltage is equal to the voltage applied to REF/2 or approximately equal to one-half of the V_{CC} when REF/2 is left open. The voltage at REF/2 should be one-half the full-scale differential input voltage between the analog inputs. Thus, the differential input voltage range when REF/2 is open and V_{CC} = 5 V is 0 V to 5 V. $V_{REF/2}$ for an input voltage range from 0.5 V to 3.5 V (full-scale differential voltage of 3 V) is 1.5 V.
4. These values are with respect to DGTL GND.
5. Total unadjusted error is specified only at an f_{clock} of 640 kHz with a duty cycle of 40% to 60% (pulse duration 625 ns to 937 ns). For frequencies above this limit or pulse duration below 625 ns, error may increase. The duty cycle limits should be observed for an f_{clock} greater than 640 kHz. Below 640 kHz, this duty cycle limit can be exceeded provided $t_{w(CLK)}$ remains within limits

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, f_{clock} = 640 kHz, $V_{REF/2}$ = 2.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			V
		DB and $\overline{INTR}$	V_{CC} = 4.75 V,	I_{OH} = −10 μA	4.5			
V_{OL}	Low-level output voltage	Data outputs	V_{CC} = 4.75 V,	I_{OL} = 1.6 mA			0.4	V
		$\overline{INTR}$ output	V_{CC} = 4.75 V,	I_{OL} = 1 mA			0.4	
		CLK OUT	V_{CC} = 4.75 V,	I_{OL} = 360 μA			0.4	
V_{T+}	Clock positive-going threshold voltage				2.7	3.1	3.5	V
V_{T-}	Clock negative-going threshold voltage				1.5	1.8	2.1	V
$V_{T+} - V_{T-}$	Clock input hysteresis				0.6	1.3	2	V
I_{IH}	High-level input current					0.005	1	μA
I_{IL}	Low-level input current					−0.005	−1	μA
I_{OZ}	Off-state output current		V_O = 0,				−3	μA
			V_O = 5 V				3	
I_{OHS}	Short-current output current	Output high	V_O = 0,	T_A = 25°C	−4.5	−6		mA
I_{OLS}	Short-circuit output current	Output low	V_O = 5 V,	T_A = 25°C	9	16		mA
I_{CC}	Supply current plus reference current		$V_{REF/2}$ = open, $\overline{CS}$ = 5 V	T_A = 25°C,		1.1	1.8	mA
$R_{REF/2}$	Input resistance to reference ladder		See Note 6		2.5	8		kΩ
C_i	Input capacitance (control)					5	7.5	pF
C_o	Output capacitance (DB)					5	7.5	pF

NOTE 6: Resistance is calculated from the current drawn from a 5-V supply applied to pins 8 and 9.

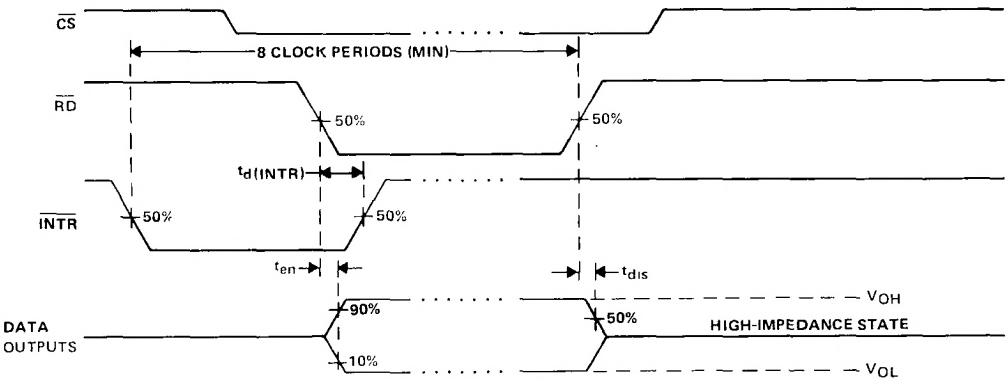
operating characteristics over recommended operating free-air temperature, V_{CC} = 5 V, $V_{REF/2}$ = 2.5 V, f_{clock} = 640 kHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Supply-voltage-variation error		V_{CC} = 4.5 V to 5.5 V,	See Note 7		±1/16	±1/8	LSB
	Total adjusted error	ADC0803	With full-scale adjust,	See Notes 7 and 8			±1/4	LSB
							±1/2	
	Total unadjusted error	ADC0805	$V_{REF/2}$ = 2.5 V,	See Notes 7 and 8			±1/2	LSB
			$V_{REF/2}$ open,	See Notes 7 and 8			±1	
	DC common-mode error		See Notes 7 and 8			±1/16	±1/8	LSB
t_{en}	Output enable time		T_A = 25°C,	C_L = 100 pF		135	200	ns
t_{dis}	Output disable time		T_A = 25°C, C_L = 10 pF,	R_L = 10 kΩ		125	200	ns
$t_{d(INTR)}$	Delay time to reset $\overline{INTR}$		T_A = 25°C			300	450	ns
t_{conv}	Conversion cycle time		f_{clock} = 100 kHz to 1.46 MHz, T_A = 25°C,	See Note 9	66		73	clock cycles
CR	Free-running conversion rate		$\overline{INTR}$ connected to $\overline{WR}$,	$\overline{CS}$ at 0 V			8770	conv/s

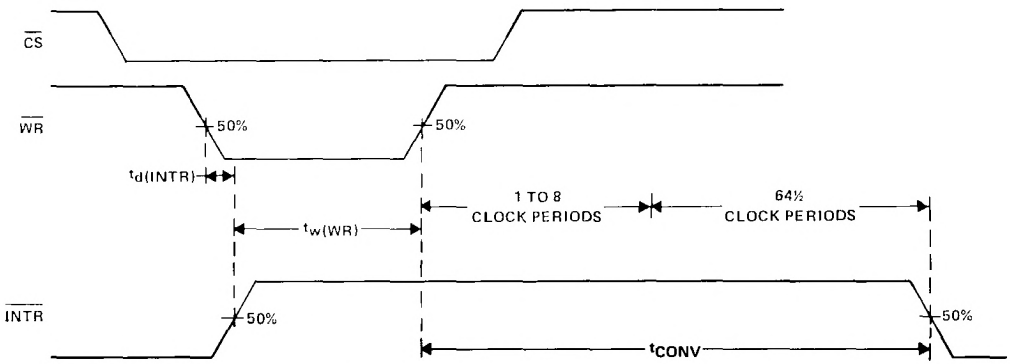
†All typical values are at T_A = 25°C.

NOTES: 7. These parameters are specified over the recommended analog input voltage range.
8. All errors are measured with reference to an ideal straight line through the end-points of the analog-to-digital transfer characteristic.
9. Although internal conversion is completed in 64 clock periods, a $\overline{CS}$ or $\overline{WR}$ low-to-high transition is followed by 1 to 8 clock periods before conversion starts. After conversion is complete, part of another clock period is required before a high-to-low transition of $\overline{INTR}$ completes the cycle.

PARAMETER MEASUREMENT INFORMATION



READ OPERATION TIMING DIAGRAM



WRITE OPERATION TIMING DIAGRAM

PRINCIPLES OF OPERATION

The ADC0803 and ADC0805 each contain a circuit equivalent to a 256-resistor network. Analog switches are sequenced by successive-approximation logic to match an analog differential input voltage ($V_{in+} - V_{in-}$) to a corresponding tap on the 256R network. The most significant bit (MSB) is tested first. After eight comparisons (64 clock periods), an eight-bit binary code (1111 1111 = full scale) is transferred to an output latch and the interrupt ($\overline{INTR}$) output goes low. The device can be operated in a free-running mode by connecting the $\overline{INTR}$ output to the write ($\overline{WR}$) input and holding the conversion start ($\overline{CS}$) input at a low level. To re start-up under all conditions, a low-level $\overline{WR}$ input is required during the power-up cycle. Taking low any time after that will interrupt a conversion in process.

When the $\overline{WR}$ input goes low, the internal successive approximation register (SAR) and 8-bit shift register are reset. As long as both $\overline{CS}$ and $\overline{WR}$ remain low, the analog-to-digital converter remains in a reset state. One to eight clock periods after $\overline{CS}$ or $\overline{WR}$ makes a low-to-high transition, conversion starts.

When the $\overline{CS}$ and $\overline{WR}$ inputs are low, the start flip-flop is set and the interrupt flip-flop and 8-bit register are reset. The next clock pulse transfers a logic high to the output of the start flip-flop. The logic high is ANDed with the next clock pulse, placing a logic high on the reset input of the start flip-flop. If either $\overline{CS}$ or $\overline{WR}$ have gone high, the set signal to the start flip-flop is removed, causing it to be reset. A logic high is placed on the D input of the eight-bit shift register and the conversion process is started. If the $\overline{CS}$ and $\overline{WR}$ inputs are still low, the start flip-flop, the 8-bit shift register, and the SAR remain reset. This action allows for wide $\overline{CS}$ and $\overline{WR}$ inputs, with conversion starting from one to eight clock periods after one of the inputs goes high.

When the logic high input has been clocked through the 8-bit shift register, which completes the SAR search, it is applied to an AND gate controlling the output latches and to the D input of a flip-flop. On the next clock pulse, the digital word is transferred to the 3-state output latches and the interrupt flip-flop is set. The output of the interrupt flip-flop is inverted to provide an $\overline{INTR}$ output that is high during conversion and low when the conversion is complete.

When a low is at both the $\overline{CS}$ and $\overline{RD}$ inputs, an output is applied to the DB0 through DB7 outputs and the interrupt flip-flop is reset. When either the $\overline{CS}$ or $\overline{RD}$ inputs return to a high state, the DB0 through DB7 outputs are disabled (returned to the high-impedance state). The interrupt flip-flop remains reset.

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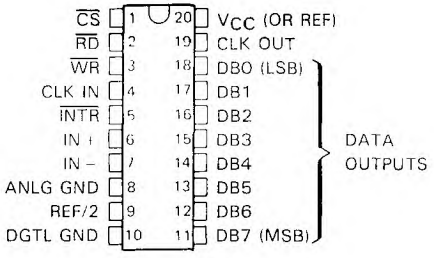
- 8-Bit Resolution
- Ratiometric Conversion
- 100-μs Conversion Time
- 135-ns Access Time
- No Zero Adjust Requirement
- On-Chip Clock Generator
- Single 5-V Power Supply
- Operates with Microprocessor or as Stand-Alone
- Designed to be Interchangeable with National Semiconductor and Signetics ADC0804

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



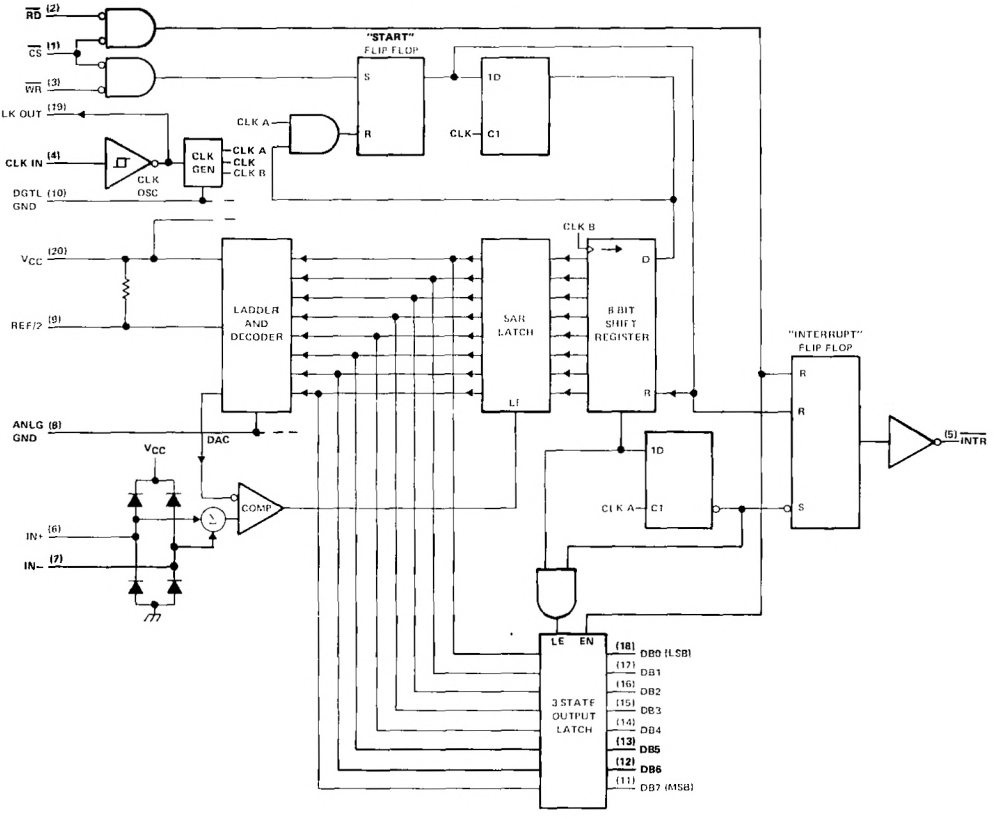
description

The ADC0804 is a CMOS 8-bit successive-approximation analog-to-digital converter that uses a modified potentiometric (256R) ladder. The ADC0804 is designed to operate from common microprocessor control buses, with the three-state output latches driving the data bus. The ADC0804 can be made to appear to the microprocessor as a memory location or an I/O port. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

A differential analog voltage input allows increased common-mode rejection and offset of the zero-input analog voltage value. Although a reference input (REF/2) is available to allow 8-bit conversion over smaller analog voltage spans or to make use of an external reference, ratiometric conversion is possible with the REF/2 input open. Without an external reference, the conversion takes place over a span from V_{CC} to analog ground (ANLG GND). The ADC0804 can operate with an external clock signal or, with an additional resistor and capacitor, can operate using an on-chip clock generator.

The ADC0804I is characterized for operation from −40 °C to 85 °C. The ADC0804C is characterized for operation from 0 °C to 70 °C.

functional block diagram (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ . . . . . −0.3 V to 18 V
other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range: ADC0804I . . . . . −40°C to 85°C
ADC0804C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to digital ground (DGTL GND) with DGTL GND and ANLG GND connected together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	6.3	V
Voltage at REF/2, $V_{REF/2}$ (see Note 2)		0.25	2.5		V
High-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$, V_{IH}		2		15	V
Low-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$, V_{IL}				0.8	V
Analog ground voltage (see Note 3)		−0.05	0	1	V
Analog input voltage (see Note 4)		−0.05		V_{CC}+0	V
Clock input frequency, f_{clock} (see Note 5)		100	640	1460	kHz
Duty cycle for $f_{clock} \geq 640$ kHz (see Note 5)		40		60	%
Pulse duration clock input (high or low) for $f_{clock} < 640$ kHz, $t_{w(CLK)}$ (see Note 5)		275	781		ns
Pulse duration, $\overline{WR}$ input low (start conversion), $t_{w(WR)}$		100			ns
Operating free-air temperature, T_A	ADC0804I	−40		85	°C
	ADC0804C	0		70	

NOTES: 2. The internal reference voltage is equal to the voltage applied to REF/2, or approximately equal to one-half of the V_{CC} when REF/2 is left open. The voltage at REF/2 should be one-half the full-scale differential input voltage between the analog inputs. Thus, the differential input voltage when REF/2 is open and V_{CC} = 5 V is 0 to 5 V. VREF/2 for an input voltage range from 0.5 V to 3.5 V (full-scale differential voltage of 3 V) is 1.5 V.
3. These values are with respect to DGTL GND.
4. When the differential input voltage ($V_{IN+} - V_{in-}$) is less than or equal to 0 V, the output code is 0000 0000.
5. Total unadjusted error is specified only at an f_{clock} of 640 kHz with a duty cycle of 40% to 60% (pulse duration 625 ns to 937 ns). For frequencies above this limit or pulse duration below 625 ns, error may increase. The duty cycle limits should be observed for an f_{clock} greater than 640 kHz. Below 640 kHz, this duty cycle limit can be exceeded provided $t_{w(CLK)}$ remains within limits.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, f_{clock} = 640 kHz, REF/2 = 2.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.75 V, I_{OH} = −360 μA	2.4			V
		DB and $\overline{INTR}$	V_{CC} = 4.75 V, I_{OH} = −10 μA	4.5			
V_{OL}	Low-level output voltage	Data outputs	V_{CC} = 4.75 V, I_{OL} = 1.6 mA			0.4	V
		$\overline{INTR}$ output	V_{CC} = 4.75 V, I_{OL} = 1 mA			0.4	
		CLK OUT	V_{CC} = 4.75 V, I_{OL} = 360 μA			0.4	
V_{T+}	Clock positive-going threshold voltage			2.7	3.1	3.5	V
V_{T-}	Clock negative-going threshold voltage			1.5	1.8	2.1	V
$V_{T+} - V_{T-}$	Clock input hysteresis			0.6	1.3	2	V
I_{IH}	High-level input current				0.005	1	μA
I_{IL}	Low-level input current				−0.005	−1	μA
I_{OZ}	Off-state output current		V_O = 0			−3	μA
			V_O = 5 V			3	
I_{OHS}	Short-circuit output current	Output high	V_O = 0, T_A = 25°C	−4.5	−6		mA
I_{OLS}	Short-circuit output current	Output low	V_O = 5 V, T_A = 25°C	9	16		mA
I_{CC}	Supply current plus reference current		REF/2 open, $\overline{CS}$ at 5 V, T_A = 25°C		1.9	2.5	mA
$R_{REF/2}$	Input resistance to reference ladder		See Note 6	1	1.3		kΩ
C_i	Input capacitance (	)			5	7.5	pF
C_o	Output capacitance				5	7.5	pF

operating characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, $V_{REF/2}$ = 2.5 V, f_{clock} = 640 kHz (unless otherwise noted)

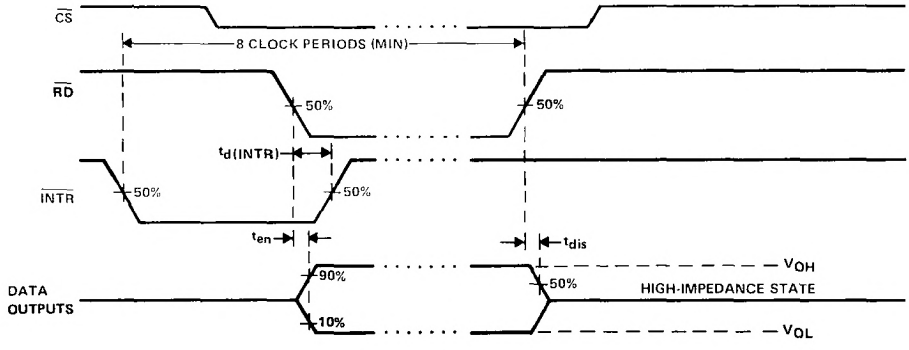
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Supply-voltage-variation error (See Notes 2 and 7)	V_{CC} = 4.5 V to 5.5 V		±1/16	±1/8	LSB
	Total unadjusted error (See Notes 7 and 8)	$V_{REF/2}$ = 2.5 V			±1	LSB
	DC common-mode error (See Note 8)			±1/16	±1/8	LSB
t_{en}	Output enable time	C_L = 100 pF		135	200	ns
t_{dis}	Output disable time	C_L = 10 pF, R_L = 10 kΩ		125	200	ns
$t_{d(INTR)}$	Delay time to reset			300	450	ns
t_{conv}	Conversion cycle time (See Note 9)	f_{clock} = 100 kHz to 1.46 MHz	65½		72½	clock cycles
	Conversion time		103		114	μs
CR	Free-running conversion rate	$\overline{INTR}$ connected to $\overline{WR}$, $\overline{CS}$ at 0 V			8827	conv/s

†All typical values are at T_A = 25°C.

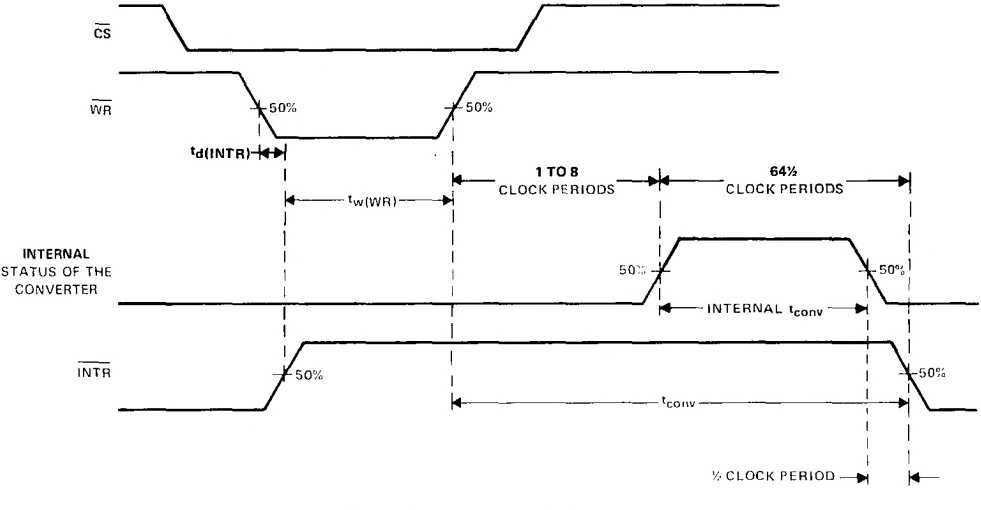
NOTES: 2. The internal reference voltage is equal to the voltage applied to REF/2, or approximately equal to one-half of the V_{CC} when REF/2 is left open. The voltage at REF/2 should be one-half the full-scale differential input voltage between the analog inputs. Thus, the differential input voltage when REF/2 is open and V_{CC} = 5 V is 0 to 5 V. $V_{REF/2}$ for an input voltage range from 0.5 V to 3.5 V (full-scale differential voltage of 3 V) is 1.5 V.

6. The resistance is calculated from the current drawn from a 5-V supply applied to pins 8 and 9.
7. These parameters are specified for the recommended analog input voltage range.
8. All errors are measured with reference to an ideal straight line through the end-points of the analog-to-digital transfer characteristic.
9. Although internal conversion is completed in 64 clock periods, a $\overline{CS}$ or $\overline{WR}$ low-to-high transition is followed by 1 to 8 clock periods before conversion starts. After conversion is completed, part of another clock period is required before a high-to-low transition of $\overline{INTR}$ completes the cycle.

timing diagrams



READ OPERATION TIMING DIAGRAM



WRITE OPERATION TIMING DIAGRAM

PRINCIPLES OF OPERATION

The ADC0804 contains a circuit equivalent to a 256-resistor network. Analog switches are sequenced by successive approximation logic to match an analog differential input voltage ($V_{in+} - V_{in-}$) to a corresponding tap on the 256-resistor network. The most-significant bit (MSB) is tested first. After eight comparisons (64 clock periods), an 8-bit binary code (1111 1111 = full scale) is transferred to an output latch and the interrupt ($\overline{INTR}$) output goes low. The device can be operated in a free-running mode by connecting the $\overline{INTR}$ output to the write ($\overline{WR}$) input and holding the conversion start ($\overline{CS}$) input at a low level. To ensure start-up under all conditions, a low-level $\overline{WR}$ input is required during the power-up cycle. Taking $\overline{CS}$ low anytime after that will interrupt a conversion in process.

When the $\overline{WR}$ input goes low, the ADC0804 successive approximation register (SAR) and 8-bit shift register are reset. As long as both $\overline{CS}$ and $\overline{WR}$ remain low, the ADC0804 remains in a reset state. One to eight clock periods after $\overline{CS}$ or $\overline{WR}$ makes a low-to-high transition, conversion starts.

When the $\overline{CS}$ and $\overline{WR}$ inputs are low, the start flip-flop is set and the interrupt flip-flop and 8-bit register are reset. The next clock pulse transfers a logic high to the output of the start flip-flop. The logic high is ANDed with the next clock pulse, placing a logic high on the reset input of the start flip-flop. If either $\overline{CS}$ or $\overline{WR}$ have gone high, the set signal to the start flip-flop is removed, causing it to be reset. A logic high is placed on the D input of the 8-bit shift register and the conversion process is started. If the $\overline{CS}$ and $\overline{WR}$ inputs are still low, the · ··· flip-flop, the 8-bit shift register, and the SAR remain reset. This action allows for wide $\overline{CS}$ and ∴ · inputs with conversion starting from one to eight clock periods after one of the inputs goes high.

When the logic high input has been clocked through the 8-bit shift register, completing the SAR search, it is applied to an AND gate controlling the output latches and to the D input of a flip-flop. On the next clock pulse, the digital word is transferred to the three-state output latches and the interrupt flip-flop is set. The output of the interrupt flip-flop is inverted to provide an $\overline{INTR}$ output that is high during conversion and low when the conversion is completed.

When a low is at both the $\overline{CS}$ and $\overline{RD}$ inputs, an output is applied to the DB0 through DB7 outputs and the interrupt flip-flop is reset. When either the $\overline{CS}$ or $\overline{RD}$ inputs return to a high state, the DB0 through DB7 outputs are disabled (returned to the high-impedance state). The interrupt flip-flop remains reset.

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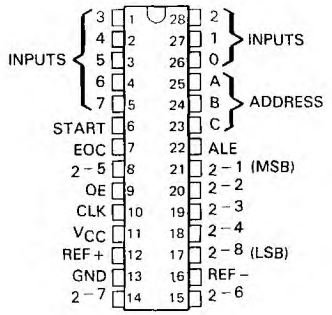
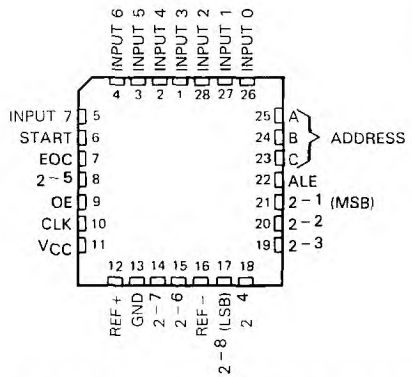
D2642, JUNE 1981–REVISED MAY 1988

- **Total Unadjusted Error . . . ±0.75 LSB Max for ADC0808 and ±1.25 LSB Max for ADC0809**
- **Resolution of 8 Bits**
- **100 μs Conversion Time**
- **Ratiometric Conversion**
- **Monotonicity Over the Entire A/D Conversion Range**
- **No Missing Codes**
- **Easy Interface with Microprocessors**
- **Latched 3-State Outputs**
- **Latched Address Inputs**
- **Single 5-V Supply**
- **Low Power Consumption**
- **Designed to be Interchangeable with National Semiconductor ADC0808, ADC0809**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



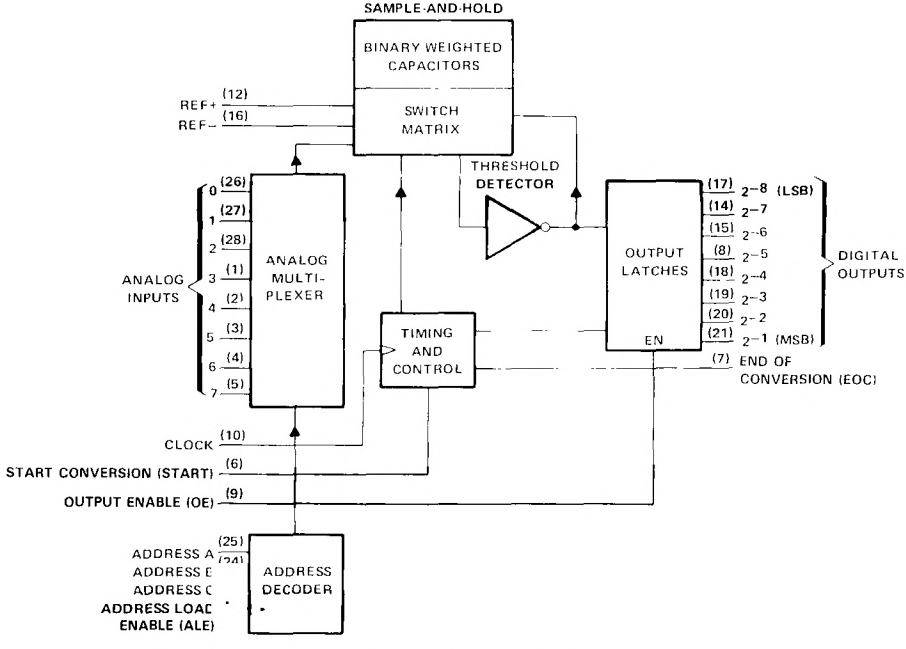
description

The ADC0808 and ADC0809 are monolithic CMOS devices with an 8-channel multiplexer, an 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to the comparator. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a switched-capacitor array, a sample-and-hold, and a successive-approximation register (SAR). Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The comparison and converting methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs from the SAR and latched inputs to the multiplexer address decoder. The single 5-V supply and low power requirements make the ADC0808 and ADC0809 especially useful for a wide variety of applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

The ADC0808 and ADC0809 are characterized for operation from −40°C to 85°C.

functional block diagram (positive logic)

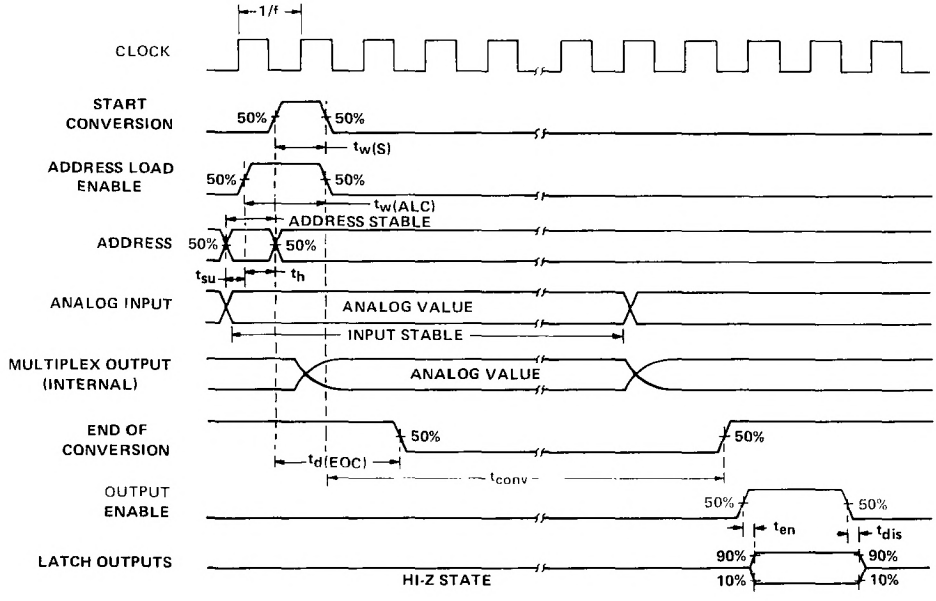


MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low-to-high transition

operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: control inputs . . . . . −0.3 to 15 V
all other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	6	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{ref-}		0	−0.1	V
Differential reference voltage, $V_{ref+} - V_{ref-}$		5		V
High-level input voltage, V_{IH}	V_{CC}−1.5			V
Low-level input voltage, V_{IL}			1.5	V
Operating free-air temperature, T_A	−40		85	°C

NOTE 2: Care must be taken that this rating is observed even during power-up.

electrical characteristics over recommended operating free-air temperature range. V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

total device

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_O = −360 μA	V_{CC}−0.4			V
V_{OL}	Low-level output voltage	Data outputs	I_O = 1.6 mA			0.45	V
		End of conversion	I_O = 1.2 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current		V_O = V_{CC}			3	μA
			V_O = 0			−3	
I_I	Control input current at maximum input voltage		V_I = 15 V			1	μA
I_{IL}	Low-level control input current		V_I = 0			−1	μA
I_{CC}	Supply current		f_{clock} = 640 kHz		0.3	3	mA
C_i	Input capacitance, control inputs		T_A = 25°C		10	15	pF
C_o	Output capacitance, data outputs		T_A = 25°C		10	15	pF
	Resistance from pin 12 to pin 16						kΩ

analog multiplexer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{on}	Channel on-state current (see Note 3)	V_I = V_{CC},	f_{clock} = 640 kHz			2	μA
		V_I = 0.1 V,	f_{clock} = 640 kHz			−2	
I_{off}	Channel off-state current	V_{CC} = 5 V, T_A = 25°C	V_I = 5 V		10		nA
			V_I = 0		−10		
		V_{CC} = 5 V	V_I = 5 V			1	μA
			V_I = 0			−1	

†Typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 3: Channel on-state current is primarily due to the bias current into or out of the threshold detector, and it varies directly with clock frequency.

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timing requirements, $V_{CC} = V_{ref+} = 5$ V, $V_{ref-} = 0$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency		10	640	1280	kHz
t_{conv}	Conversion time	See Note 4	90	100	116	μs
$t_{w(s)}$	Pulse duration, START		200			ns
$t_{w(ALE)}$	Pulse duration, ALE		200			ns
t_{su}	Setup time, ADDRESS		50			ns
t_h	Hold time, ADDRESS		50			ns
t_d	Delay time, EOC	See Notes 4 and 5	0		14.5	μs

operating characteristics, $T_A = 25°C$, $V_{CC} = V_{ref+} = 5$ V, $V_{ref-} = 0$ V, $f_{clock} = 640$ kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADC0808			ADC0809			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
k_{SVS}	Supply voltage sensitivity	$V_{CC} = V_{ref+} = 4.75$ V to 5.25 V, $T_A = -40°C$ to 85°C, See Note 6		±0.05			±0.05		%/V
	Linearity error (see Note 7)			±0.25			±0.5		LSB
	Zero error (see Note 8)			±0.25			±0.25		LSB
	Total unadjusted error (See Note 9)	$T_A = 25°C$		±0.25	±0.5		±0.5		LSB
		$T_A = -40°C$ to 85°C			±0.75			±1.25	
		$T_A = 0°C$ to 70°C						±1	
t_{en}	Output enable time	$C_L = 50$ pF, $R_L = 10$ kΩ		80	250		80	250	ns
t_{dis}	Output disable time	$C_L = 10$ pF, $R_L = 10$ kΩ		105	250		105	250	ns

†Typical values for all except supply voltage sensitivity are at $V_{CC} = 5$ V, and all are at $T_A = 25°C$.

NOTES: 4. Refer to the operating sequence diagram.
5. For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock periods plus 2 μs.
6. Supply voltage sensitivity relates to the ability of an analog-to-digital converter to maintain accuracy as the supply voltage varies. The supply and V_{ref+} are varied together and the change in accuracy is measured with respect to full-scale.
7. Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.
8. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
9. Total unadjusted error is the maximum sum of linearity error, zero error, and full-scale error

PRINCIPLES OF OPERATION

The ADC0808 and ADC0809 each consists of an analog signal multiplexer, an 8-bit successive-approximation converter, and related control and output circuitry.

multiplexer

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the address decoder. Address load control loads the address code into the decoder on a low-to-high transition. The output latch is reset by the positive-going edge of the start pulse. Sampling also starts with the positive-going edge of the start pulse and lasts for 32 clock periods. The conversion process may be interrupted by a new start pulse before the end of 64 clock periods. The previous data will be lost if a new start of conversion occurs before the 64th clock pulse. Continuous conversion may be accomplished by connecting the End-of-Conversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 1). In the first phase of the conversion process, the analog input is sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 of this capacitor is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF−. If the voltage at the summing node is greater than the trip-point of the threshold detector (approximately one-half the V_{CC} voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF−. If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF+ through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are counted.

With each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is successive approximation, but relies on charge redistribution rather than a successive-approximation register (and reference DAC) to count and weigh the bits from MSB to LSB.

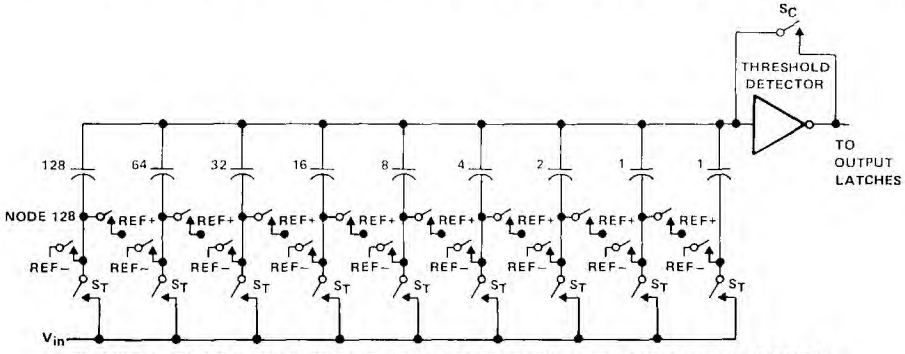
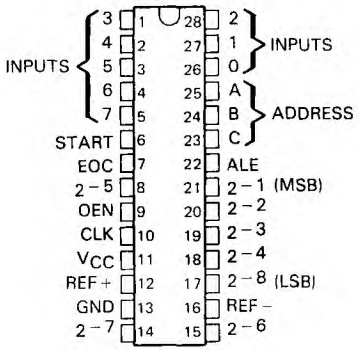


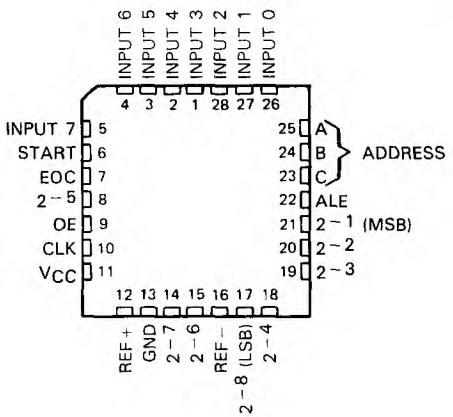
FIGURE 1. SIMPLIFIED MODEL OF THE SUCCESSIVE-APPROXIMATION SYSTEM

- **Total Unadjusted Error . . . ±0.75 LSB Max**
- **Resolution of 8 Bits**
- **100 μs Conversion Time**
- **Ratiometric Conversion**
- **Monotonous Over the Entire A/D Conversion Range**
- **No Missing Codes**
- **Easy Interface with Microprocessors**
- **Latched 3-State Outputs**
- **Latched Address Inputs**
- **Single 5-Volt Supply**
- **Low Power Consumption**
- **Designed to be Interchangeable with National Semiconductor ADC0808CJ**

J
DUAL-IN-LINE PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



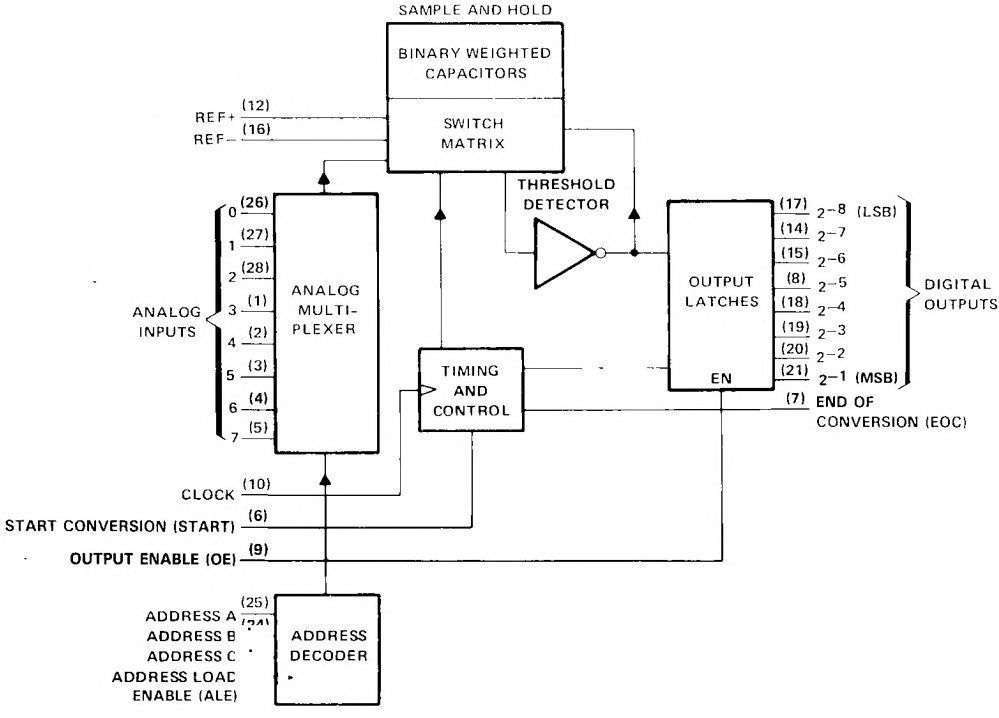
description

The ADC0808M is a monolithic CMOS device with an 8-channel multiplexer, an 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to the comparator. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a switched capacitor array, a sample-and-hold, and a successive-approximation register (SAR). Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The comparison and converting methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs from the SAR and latched inputs to the multiplexer address decoder. The single 5-volt supply and low power requirements make the ADC0808M especially useful for a wide variety of applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

The ADC0808M is characterized for operation over the full military temperature range of −55°C to 125°C.

functional block diagram (positive logic)

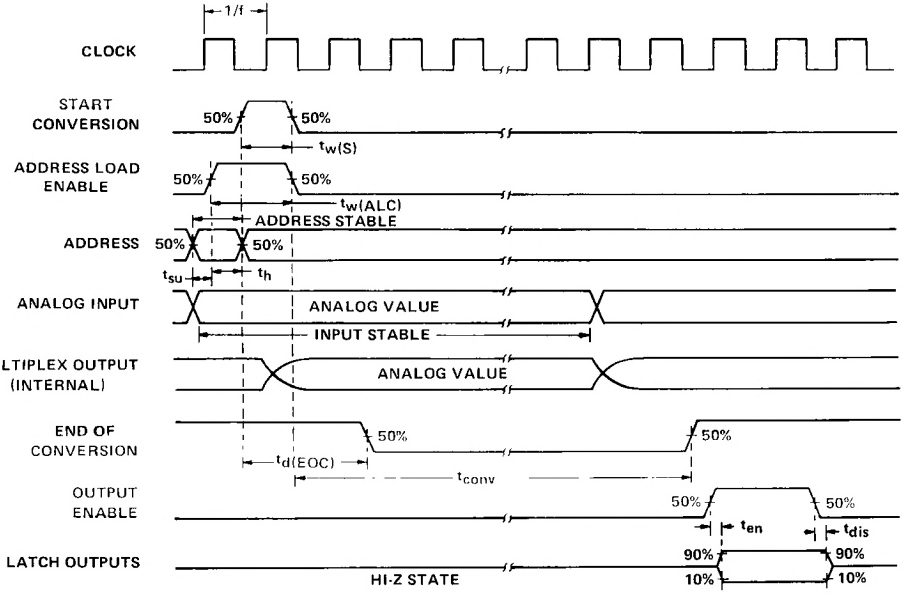


MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low to high transition

operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: control inputs . . . . . −0.3 to 15 V
all other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	6	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{ref-}		0	−0.1	V
Differential reference voltage, $V_{ref+} - V_{ref-}$		5		V
High-level input voltage, V_{IH}	V_{CC}−1.5			V
Low-level input voltage, V_{IL}			1.5	V
Start pulse duration, $t_{w(S)}$				ns
Address load control pulse duration, $t_{w(ALC)}$				ns
Address setup time, t_{su}	50			ns
Address hold time, t_h	50			ns
Clock frequency, f_{clock}	10	640	1280	kHz
Operating free-air temperature, T_A	−55		125	°C

NOTE 2: Care must be taken that this rating is observed even during power-up

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 4.5 V to 5.5 V (unless otherwise noted)

total device

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_O = −360 μA	V_{CC}−0.4			V
V_{OL}	Low-level output voltage	Data outputs	I_O = 1.6 mA			0.45	V
		End of conversion	I_O = 1.2 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current		V_O = V_{CC}			3	μA
			V_O = 0			−3	
I_I	Control input current at maximum input voltage		V_I = 15 V			1	μA
I_{IL}	Low-level control input current		V_I = 0			−1	μA
I_{CC}	Supply current		f_{clock} = 640 kHz		0.3	3	mA
C_i	Input capacitance, control inputs		T_A = 25°C		10		pF
C_o	Output capacitance, data outputs		T_A = 25°C		10		pF
	Resistance from pin 12 to pin 16						kΩ

analog multiplexer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{on}	Channel on-state current (see Note 3)	V_I = V_{CC},	f_{clock} = 640 kHz			2	μA
		V_I = 0,	f_{clock} = 640 kHz			−2	
I_{off}	Channel off-state current	V_{CC} = 5 V, T_A = 25°C	V_I = 5 V		10	200	nA
			V_I = 0		−10	−200	
		V_{CC} = 5 V	V_I = 5 V			1	μA
			V_I = 0			−1	

† Typical values are at V_{CC} = 5 V and T_A = 25°C

NOTE 3: Channel on-state current is primarily due to the bias current into or out of the threshold detector, and it varies directly with clock frequency.

timing characteristics, V_{CC} = V_{ref+} = 5 V, V_{ref-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency		10	640	1	kHz
t_{conv}	Conversion time	See Notes 4 and 5 and Figure 1	90	100	116	μs
t_{enH}	Enable time, high	See Figure 1		150		ns
t_{enL}	Enable time, low	See Figure 1		90		ns
t_{dis}	Output disable time	See Figure 1		200	405	ns
$t_{w(s)}$	Pulse duration, START		200			ns
$t_{w(ALE)}$	Pulse duration, ALE		200			ns
t_{su}	Setup time,		50			ns
t_h	Hold time, A		50			ns
$t_{d(EOC)}$	Delay time, EOC	See Notes 4 and 6 and Figure 1	0		14.5	μs

NOTES: 4. Refer to the operating sequence diagram.
5. For clock frequencies other than 640 kHz, t_{conv} is 57 clock cycles minimum and 74 clock cycles maximum.
6. For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock cycles plus 2 μs.

operating characteristics, T_A = 25°C, V_{CC} = V_{ref+} = 5 V, V_{ref-} = 0 V, f_{clock} = 640 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
k_{SVS}	Supply voltage sensitivity	V_{CC} = V_{ref+} = 4.5 V to 5.5 V, T_A = −55°C to 125°C, See Note 7		±0.05		%/V
	Linearity error (see Note 8)			±0.25		LSB
	Zero error (see Note 9)			±0.25		LSB
	Total unadjusted error (see Note 10)	T_A = 25°C		±0.25	±0.5	LSB
		T_A = −55°C to 125°C			±0.75	

† Typical values for all except supply voltage sensitivity are at V_{CC} = 5 V, and all are at T_A = 25°C.

NOTES: 7. Supply voltage sensitivity relates to the ability of an analog-to-digital converter to maintain accuracy as the supply voltage varies. The supply and V_{ref+} are varied together and the change in accuracy is measured with respect to full-scale.
8. Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.
9. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
10. Total unadjusted error is the maximum sum of linearity error, zero error, and full-scale error.

PARAMETER MEASUREMENT INFORMATION

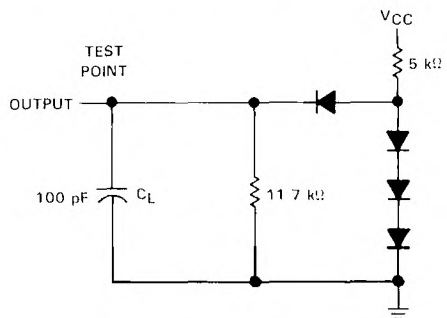


FIGURE 1. TEST CIRCUIT

TEXAS INSTRUMENTS
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PRINCIPLES OF OPERATION

The ADC0808M consists of an analog signal multiplexer, an 8-bit successive-approximation converter, and related control and output circuitry.

multiplexer

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the address decoder. Address load control loads the address code into the decoder on a low-to-high transition. The output latch is reset by the positive-going edge of the start pulse. Sampling also starts with the positive-going edge of the start pulse and lasts for 32 clock periods. The conversion process may be interrupted by a new start pulse before the end of 64 clock periods. The previous data will be lost if a new start of conversion occurs before the 64th clock pulse. Continuous conversion may be accomplished by connecting the End-of-Conversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 2). In the first phase of the conversion process, the analog input is sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 of this capacitor is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF−. If the voltage at the summing node is greater than the trip-point of the threshold detector (approximately one-half the V_{CC} voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF−. If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF+ through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are counted.

With each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is successive approximation, but relies on charge redistribution rather than a successive-approximation register (and reference DAC) to count and weigh the bits from MSB to LSB.

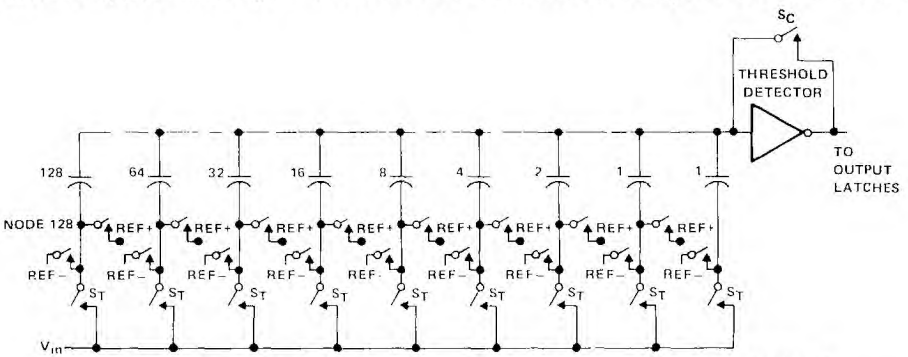


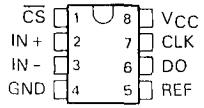
FIGURE 2. SIMPLIFIED MODEL OF THE SUCCESSIVE-APPROXIMATION SYSTEM

D2795, AUGUST 1985–REVISED JUNE 1986

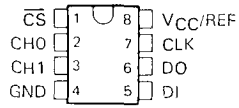
- 8-Bit Resolution
- Easy Microprocessor Interface or Stand-Alone Operation
- Operates Ratiometrically or with 5-V Reference
- Single Channel or Multiplexed Twin Channels with Single-Ended or Differential Input Options
- Input Range 0 to 5 V with Single 5-V Supply
- Inputs and Outputs are Compatible with TTL and MOS
- Conversion Time of 32 μs at CLK = 250 kHz
- Designed to be Interchangeable with National Semiconductor ADC0831 and ADC0832

DEVICE	TOTAL UNADJUSTED ERROR (SEE NOTE 1)	
	ADJUSTMENT	BEST
ADC0831	±1 LSB	±½ LSB
ADC0832	±1 LSB	±½ LSB

ADC0831 . . . P DUAL-IN-LINE PACKAGE
(TOP VIEW)



ADC0832 . . . P DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

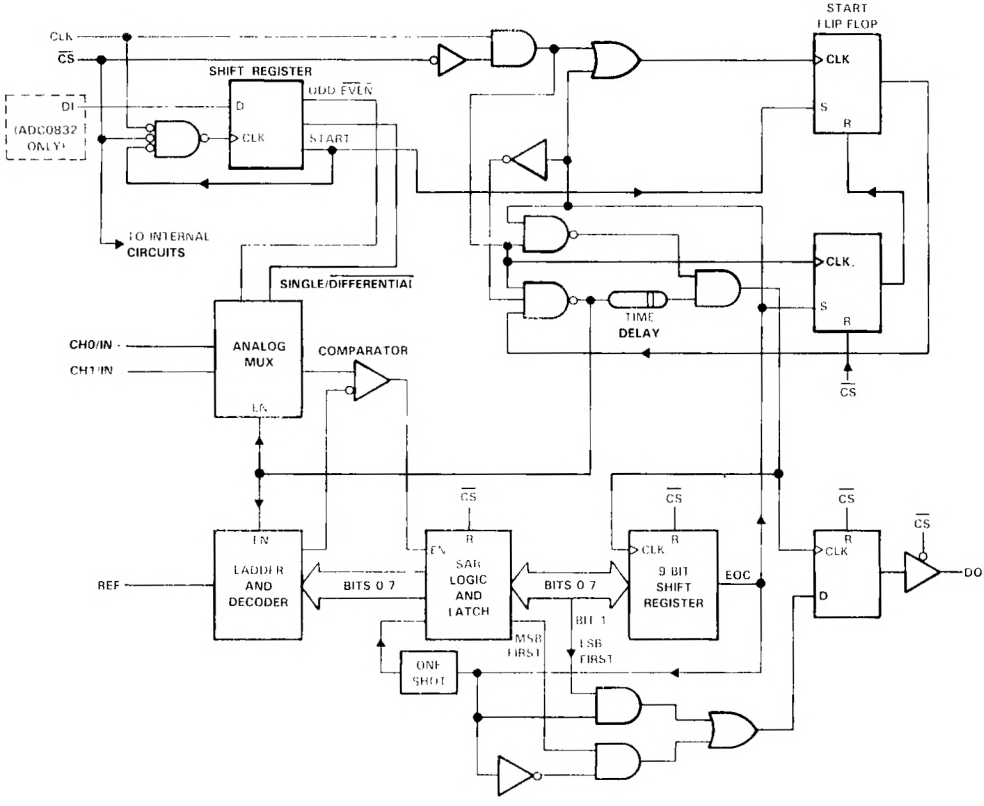
These devices are 8-bit successive-approximation analog-to-digital converters. The ADC0831A and ADC0831B have single input channels; the ADC0832A and ADC0832B have multiplexed twin input channels. The serial output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The ADC0832 multiplexer is software configured for single-ended or differential inputs. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The operation of the ADC0831 and ADC0832 devices is very similar to the more complex ADC0834 and ADC0838 devices. Ratiometric conversion can be attained by setting the REF input equal to the maximum analog input signal value, which gives the highest possible conversion resolution. Typically, REF is set equal to V_{CC} (done internally on the ADC0832). For more detail on the operation of the ADC0831 and ADC0832 devices, refer to the ADC0834/ADC0838 data sheet.

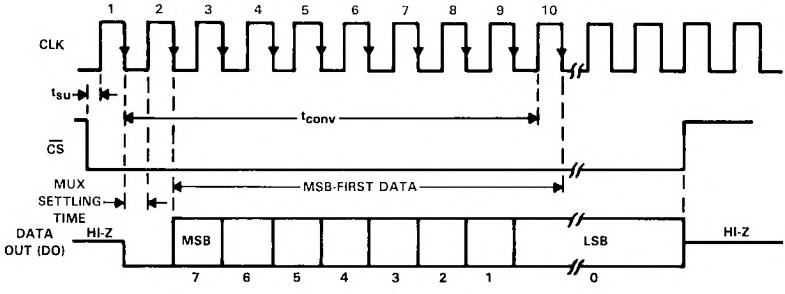
The ADC0831AI, ADC0831BI, ADC0832AI, and ADC0832BI are characterized for operation from −40°C to 85°C. The ADC0831AC, ADC0831BC, ADC0832AC, and ADC0832BC are characterized for operation from 0°C to 70°C.

functional block diagram

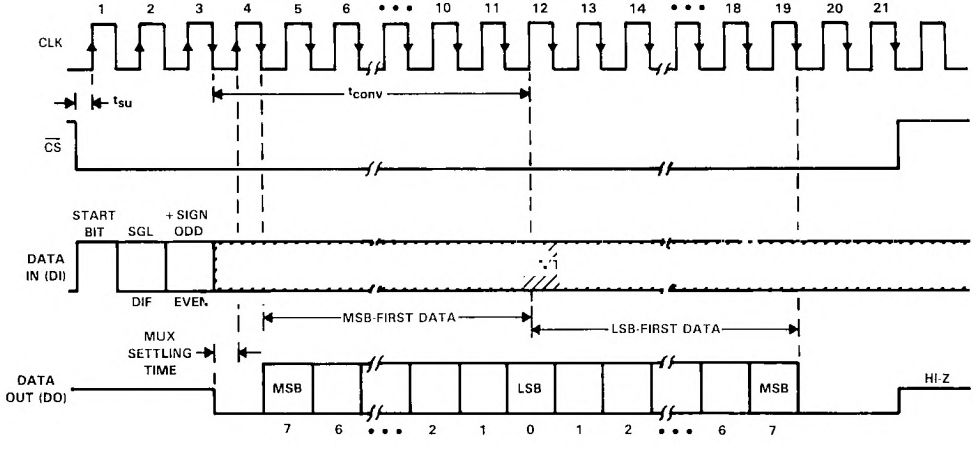


sequence of operation

ADC0831



ADC0832



ADC0832 MUX ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS		CHANNEL NUMBER	
SGL/$\overline{DIF}$	ODD/$\overline{EVEN}$	0	1
L	L	+	−
L	H	−	+
H	L	+	
H	H		+

H = high level, L = low level, − or + = polarity of selected input pin

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: Logic . . . . . −0.3 V to 15 V
Analog . . . . . −0.3 V to V_{CC} + 0.3 V
Input current . . . . . ±5 mA
Total input current for package . . . . . ±20 mA
Operating free-air temperature range: I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	6.3	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
f_{clock}	Clock frequency		10		400	kHz
	Clock duty cycle (see Note 2)		40		60	%
$t_{wH(CS)}$	Pulse duration, $\overline{CS}$ high					ns
t_{su}	Setup time, $\overline{CS}$ low or ADC0832 data valid before clock↑					ns
t_h	Hold time, ADC0832 data valid after clock↑		90			ns
T_A	Operating free-air temperature	I-suffix	−40		85	°C
		C-suffix	0		70	

NOTE 2: The clock duty cycle range ensures proper operation at all clock frequencies. If a clock frequency is used outside the recommended duty cycle range, the minimum pulse duration (high or low) is 1 μs.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

digital section

PARAMETER		TEST CONDITIONS†	I SUFFIX			C SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, I_{OH} = −360 μA	2.4			2.8			V
		V_{CC} = 4.75 V, I_{OH} = −10 μA	4.5			4.6			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 1.6 mA	0.4			0.34			V
I_{IH}	High-level input current	V_{IH} = 5 V		0.005	1		0.005	1	μA
I_{IL}	Low-level input current	V_{IL} = 0		−0.005	−1		−0.005	−1	μA
I_{OH}	High-level output (source) current	V_{OH} = V_O, T_A = 25°C	−6.5	−14		−6.5	−14		mA
I_{OL}	Low-level output (sink) current	V_{OL} = V_{CC}, T_A = 25°C	8	16		8	16		mA
I_{OZ}	High-impedance-state output current (DO)	V_O = 5 V, T_A = 25°C		0.01	3		0.01	3	μA
		V_O = 0, T_A = 25°C		−0.01	−3		−0.01	−3	
C_i	Input capacitance			5			5		pF
C_o	Output capacitance			5			5		pF

† All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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electrical characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

analog and converter section

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{ICR}	Common-mode input voltage range		See Note 3	−0.05 to V_{CC}+0.05			V
$I_{I(stdby)}$	Standby input current (see Note 4)	On-channel	V_I = 5 V at on-channel,			1	μA
		Off-channel	V_I = 0 at off-channel			−1	
		On-channel	V_I = 0 at on-channel,			−1	
		Off-channel	V_I = 5 V at off-channel			1	
$r_{i(REF)}$	Input resistance to reference ladder			1.3	2.4	5.9	kΩ

total device

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current	ADC0831			1	2.5	mA
		ADC0832			3	5.2	

†All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 3. If channel IN− is more positive than channel IN+, the digital output code will be 0000 0000. Connected to each analog input are two on-chip diodes that will conduct forward current for analog input voltages one diode drop above V_{CC}. Care must be taken during testing at low V_{CC} levels (4.5 V) because high-level analog input voltage (5 V) can, especially at high temperatures, cause this input diode to conduct and cause errors for analog inputs that are near full-scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V to 5 V input voltage range requires a minimum V_{CC} of 4.95 V for all variations of temperature and load.

4. Standby input currents are currents going into or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state condition.

operating characteristics V_{CC} = REF = 5 V, f_{clock} = 250 kHz, $t_r = t_f$ = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS§	BI, BC SUFFIX			AI, AC SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
	Supply-voltage variation error		V_{CC} = 4.75 V to 5.25 V		±1/16	±1/4		±1/16	±1/4	LSB
	Total unadjusted error (see Note 5)		V_{ref} = 5 V, T_A = MIN to MAX			±1/2			±1	LSB
	Common-mode error		Differential mode		±1/16	±1/4		±1/16	±1/4	LSB
t_{pd}	Propagation delay time, output data after CLK↓ (see Note 6)	MSB-first data	C_L = 100 pF		650	1500		650	1500	ns
		LSB-first data			250	600		250	600	
t_{dis}	Output disable time, DO after $\overline{CS}$↑		C_L = 10 pF, R_L = 10 kΩ		125	250		125	250	ns
			C_L = 100 pF, R_L = 2 kΩ			500			500	
t_{conv}	Conversion time (multiplexer addressing time not included)					8			8	clock periods

§All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

6. The most significant-bit-first data is output directly from the comparator and therefore requires additional delay to allow for comparator response time. Least-significant-bit-first data applies only to ADC0832.

PARAMETER MEASUREMENT INFORMATION

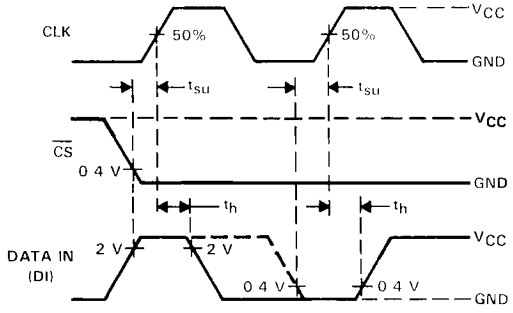


FIGURE 1. ADC0832 DATA INPUT TIMING

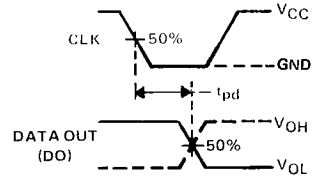
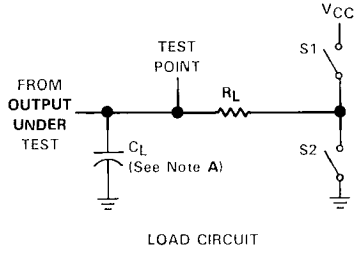
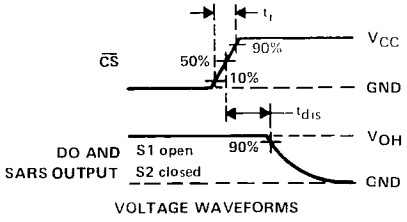


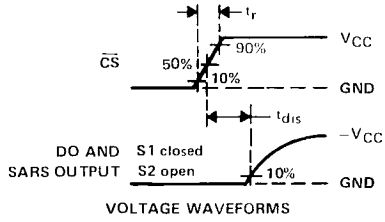
FIGURE 2. DATA OUTPUT TIMING



LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. OUTPUT DISABLE TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

UNADJUSTED OFFSET ERROR
vs
REFERENCE VOLTAGE

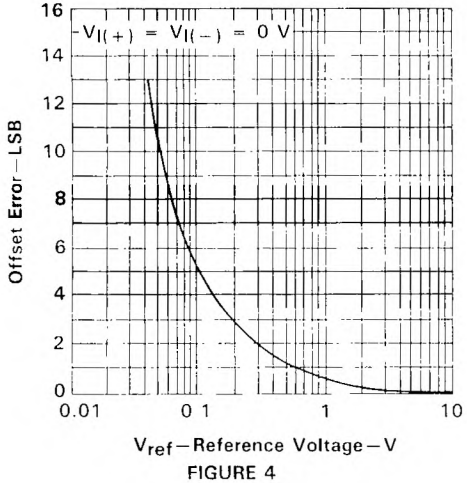


FIGURE 4

LINEARITY ERROR
vs
REFERENCE VOLTAGE

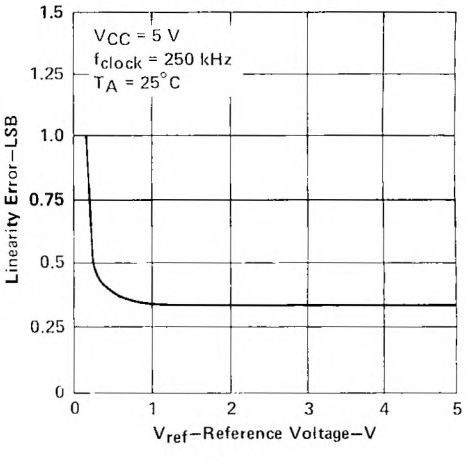


FIGURE 5

LINEARITY ERROR
vs
FREE-AIR TEMPERATURE

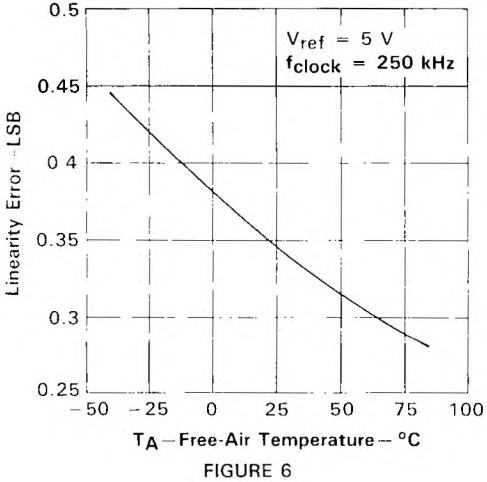


FIGURE 6

LINEARITY ERROR
vs
CLOCK FREQUENCY

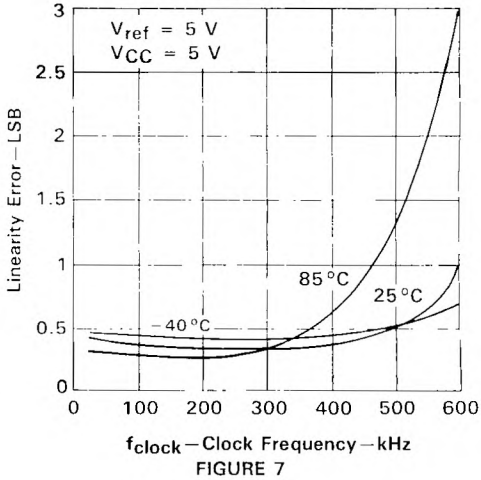


FIGURE 7

TYPICAL CHARACTERISTICS

ADC0831
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

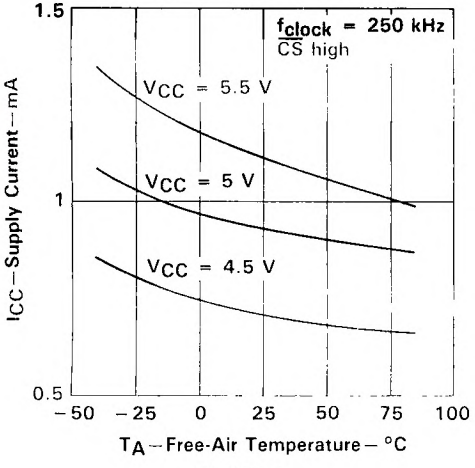


FIGURE 8

ADC0831
SUPPLY CURRENT
vs
CLOCK FREQUENCY

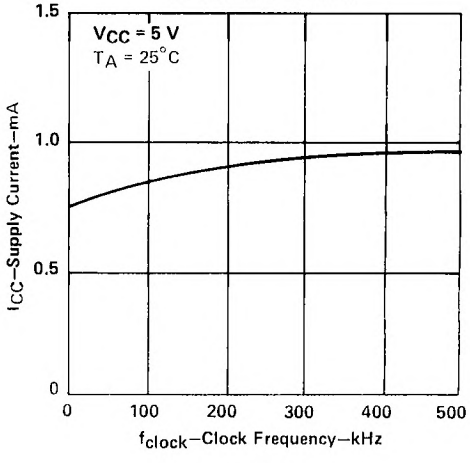


FIGURE 9

OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

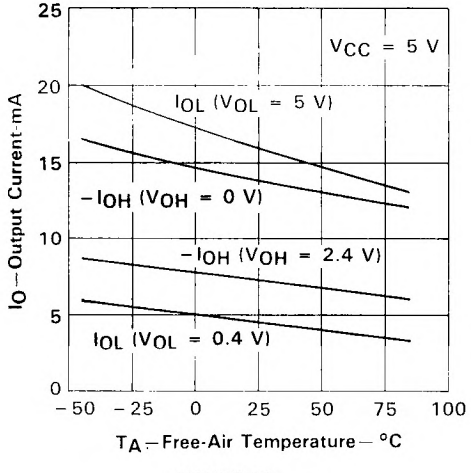


FIGURE 10

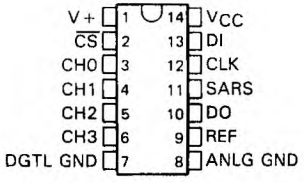
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2795, AUGUST 1985—REVISED OCTOBER 1986

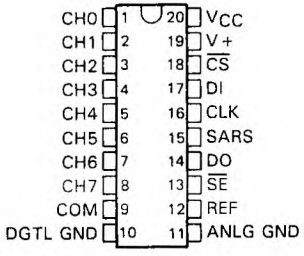
- 8-Bit Resolution
- Easy Microprocessor Interface or Stand-Alone Operation
- Operates Ratiometrically or with 5-V Reference
- 4- or 8-Channel Multiplexer Options with Address Logic
- Shunt Regulator Allows Operation with High-Voltage Supplies
- Input Range 0 to 5 V with Single 5-V Supply
- Remote Operation with Serial Data Link
- Inputs and Outputs are Compatible with TTL and MOS
- Conversion Time of 32 μs at f_{clock} = 250 kHz
- Designed to be Interchangeable with National Semiconductor ADC0834 and ADC0838

DEVICE	TOTAL UNADJUSTED ERROR	
	A SUFFIX	B SUFFIX
ADC0834	±1 LSB	±1/2 LSB
ADC0838	±1 LSB	±1/2 LSB

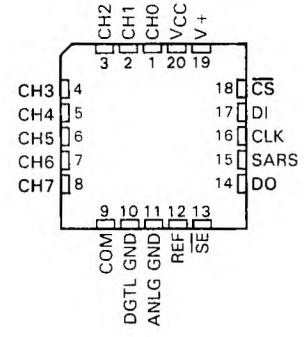
ADC0834 . . . N PACKAGE
(TOP VIEW)



ADC0838 . . . N PACKAGE
(TOP VIEW)



ADC0838 . . . FN PACKAGE
(TOP VIEW)



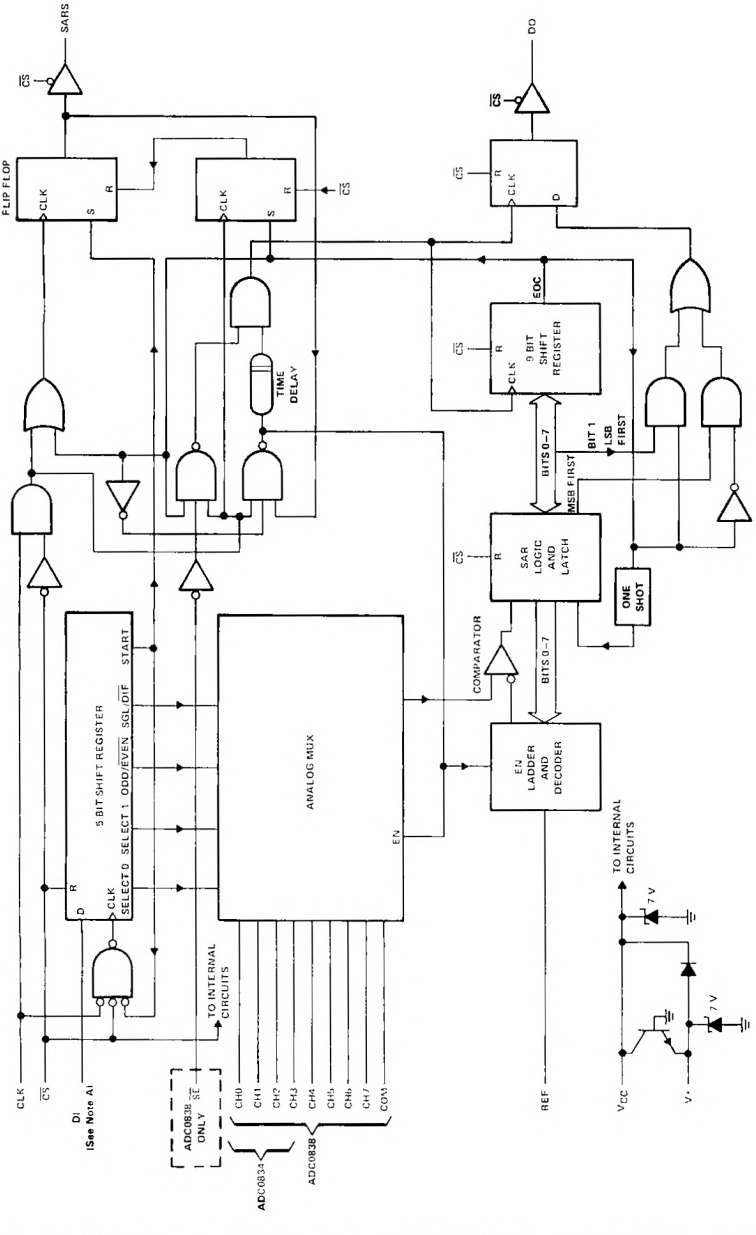
description

These devices are 8-bit successive-approximation analog-to-digital converters, each with an input-configurable multichannel multiplexer and serial input/output. The serial input/output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing with most popular microprocessors is readily available from the factory.

The ADC0834 (4-channel) and ADC0838 (8-channel) multiplexer is software configured for single-ended or differential inputs as well as pseudo-differential input assignments. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The ADC0834AI, ADC0834BI, ADC0838AI, and ADC0838BI are characterized for operation from −40°C to 85°C. The ADC0834AC, ADC0834BC, ADC0838AC, and ADC0838BC are characterized for operation from 0°C to 70°C.

functional block diagram



NOTE A: For the ADC0834, DI is input directly to the D input of SELECT 1; SELECT 0 is forced to a high.

functional description

The ADC0834 and ADC0838 use a sample data comparator structure that converts differential analog inputs by a successive-approximation routine. Operation of both devices is similar with the exception of a select enable ($\overline{SE}$) input, an analog common input, and multiplexer addressing. The input voltage to be converted is applied to a channel terminal and is compared to ground (single-ended), to an adjacent input (differential), or to a common terminal (pseudo-differential) that can be an arbitrary voltage. The input terminals are assigned a positive (+) or negative (−) polarity. If the signal input applied to the assigned positive terminal is less than the signal on the negative terminal, the converter output is all zeros.

Channel selection and input configuration are under software control using a serial data link from the controlling processor. A serial communication format allows more functions to be included in a converter package with no increase in size. In addition, it eliminates the transmission of low-level analog signals by locating the converter at the analog sensor and communicating serially with the controlling processor. This process returns noise-free digital data to the processor.

A particular input configuration is assigned during the multiplexer addressing sequence. The multiplexer address is shifted into the converter through the data input (DI) line. The multiplexer address selects the analog inputs to be enabled and determines whether the input is single-ended or differential. When the input is differential, the polarity of the channel input is assigned. Differential inputs are assigned to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a differential pair. These channels cannot act differentially with any other channel. In addition to selecting the differential mode, the polarity may also be selected. Either channel of the channel pair may be designated as the negative or positive input.

The common input on the ADC0838 can be used for a pseudo-differential input. In this mode, the voltage on the common input is considered to be the negative differential input for all channel inputs. This voltage can be any reference potential common to all channel inputs. Each channel input can then be selected as the positive differential input. This feature is useful when all analog circuits are biased to a potential other than ground.

A conversion is initiated by setting the chip select ($\overline{CS}$) input low, which enables all logic circuits. The $\overline{CS}$ input must be held low for the complete conversion process. A clock input is then received from the processor. On each low-to-high transition of the clock input, the data on the DI input is clocked into the multiplexer address shift register. The first logic high on the input is the start bit. A 3- to 4-bit assignment word follows the start bit. On each successive low-to-high transition of the clock input, the start bit and assignment word are shifted through the shift register. When the start bit is shifted into the start location of the multiplexer register, the input channel is selected and conversion starts. The SAR Status output (SARS) goes high to indicate that a conversion is in progress, and the DI input to the multiplexer shift register is disabled the duration of the conversion.

An interval of one clock period is automatically inserted to allow the selected multiplexed channel to settle. The data output DO comes out of the high-impedance state and provides a leading low for this one clock period of multiplexer settling time. The SAR comparator compares successive outputs from the resistive ladder with the incoming analog signal. The comparator output indicates whether the analog input is greater than or less than the resistive ladder output. As the conversion proceeds, conversion data is simultaneously output from the DO output pin, with the most significant bit (MSB) first.

After eight clock periods the conversion is complete and the SAR Status (SARS) output goes low.

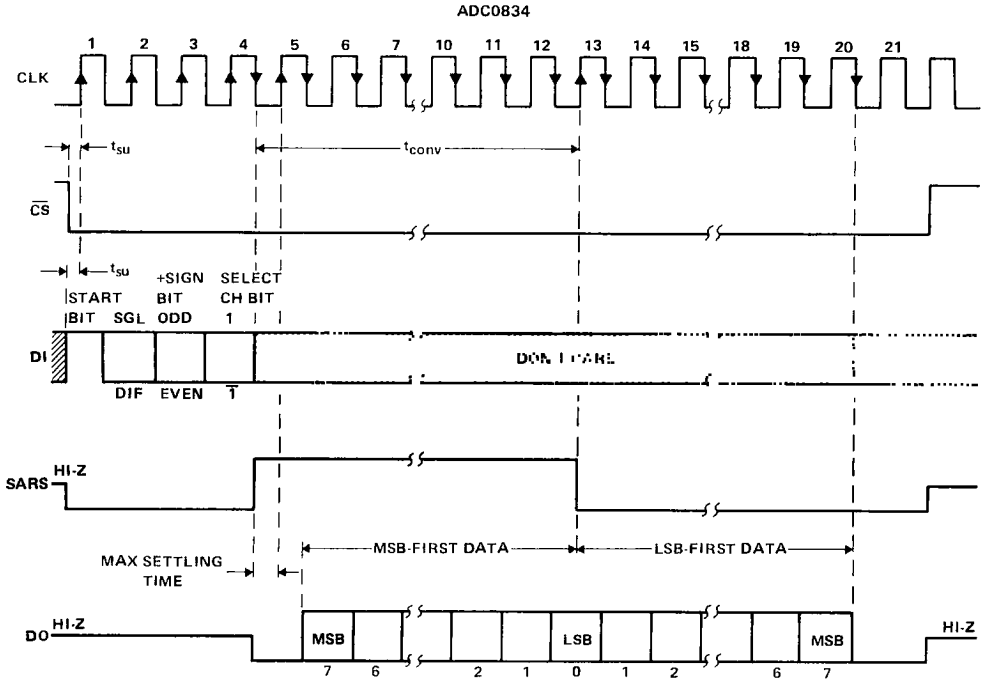
The ADC0834 outputs the least-significant-bit-first data after the MSB-first data stream. If the shift enable ($\overline{SE}$) line is held high on the ADC0838, the value of the least significant bit (LSB) will remain on the data line. When $\overline{SE}$ is forced low, the data is then clocked out as LSB-first data. (To output LSB first, the $\overline{SE}$ control input must first go low, then the data stored in the 9-bit shift register outputs LSB first.) When $\overline{CS}$ goes high, all internal registers are cleared. At this time the output circuits go to the high-impedance state. If another conversion is desired, the $\overline{CS}$ line must make a high-to-low transition followed by address information.

functional description (continued)

The DI and DO pins can be tied together and controlled by a bidirectional processor I/O bit received on a single wire. This is possible because the DI input is only examined during the multiplexer addressing interval and the DO output is still in a high-impedance state.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

sequence of operation

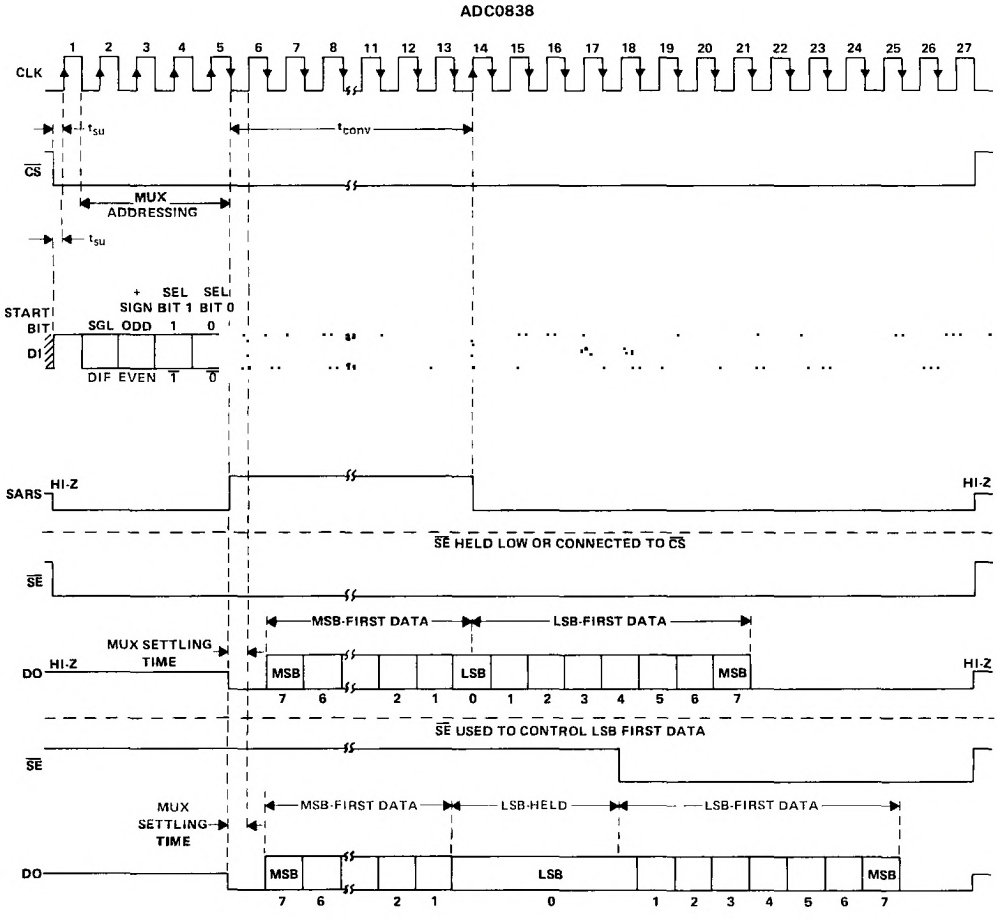


ADC0834 MUX ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS			CHANNEL NUMBER			
SGL/DIF	ODD	SELECT BIT 1	0	1	2	3
L	L	L	+	−		
L	L	H			+	−
L	H	L	−	+		
L	H	H			−	+
H	L	L	+			
H	L	H			+	
H	H	L		+		
H	H	H				+

H = high level, L = low level, − or + = polarity of selected input pin

sequence of operation



ADC0838 MUX ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS				SELECTED CHANNEL NUMBER								COM
SGL/$\overline{DIF}$	ODD/$\overline{EVEN}$	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	
L	L	L	L	+	−							
L	L	L	H				+				−	
L	L	H	L					+	−			
L	L	H	H							+	−	
L	H	L	L		+	−						
L	H	L	H				+	−				
L	H	H	L						+	−		
L	H	H	H							−	+	
H	L	L	L	+								−
H	L	L	H			+	−					−
H	L	H	L					+	−			−
H	L	H	H							+	−	−
H	H	L	L		+	−						−
H	H	L	H				+	−				
H	H	H	L						+	−		−
H	H	H	H								+	−

H = high level, L = low level, − or + = polarity of selected input

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2) . . . . . 6.5 V
Input voltage range: Logic . . . . . −0.3 V to 15 V
Analog . . . . . −0.3 V to V_{CC}+0.3 V
Input current: V+ input . . . . . 15 mA
Any other input . . . . . ±5 mA
Total input current for package . . . . . ±20 mA
Operating free-air temperature range: AI and BI suffixes . . . . . −40°C to 85°C
AC and BC suffixes . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Internal zener diodes are connected from the V_{CC} input to ground and from the V+ input to ground. The breakdown voltage of each zener diode is approximately 7 V. One zener diode can be used as a shunt regulator and connects to V_{CC} through a regular diode. When the voltage regulator powers the converter, this zener and regular diode combination ensures that the V_{CC} input (6.4 V) is less than the zener breakdown voltage. A series resistor is recommended to limit current into the V+ input.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	6.3	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
f_{clock}	Clock frequency		10		400	kHz
	Clock duty cycle (see Note 3)		40		60	%
$t_{wH(CS)}$	Pulse duration, $\overline{CS}$ high		220			ns
t_{su}	Setup time, $\overline{CS}$ low, $\overline{SE}$ low, or data valid before clock↑		350			ns
t_h	Hold time, data valid after clock↑		90			ns
T_A	Operating free-air temperature	AI and BI suffixes	−40		85	°C
		AC and BC suffixes	0		70	

NOTE 3: The clock duty cycle range ensures proper operation at all clock frequencies. If a clock frequency is used outside the recommended duty cycle range, the minimum pulse duration (high or low) is 1 μs.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = V+ = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

digital section

PARAMETER		TEST CONDITIONS†		AI, BI SUFFIX			AC, BC SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			2.8			V
		V_{CC} = 4.75 V,	I_{OH} = −10 μA	4.5			4.6			
V_{OL}	Low-level output voltage	V_{CC} = 5.25 V,	I_{OL} = 1.6 mA			0.4			0.34	V
I_{IH}	High-level input current	V_{IH} = 5 V			0.005	1		0.005	1	μA
I_{IL}	Low-level input current	V_{IL} = 0			−0.005	−1		−0.005	−1	μA
I_{OH}	High-level output (source) current	V_{OH} = 0,	T_A = 25°C	−6.5	−14		−6.5	−14		mA
I_{OL}	Low-level output (sink) current	V_{OL} = V_{CC},	T_A = 25°C	8	16		8	16		mA
I_{OZ}	High-impedance-state output current (DO or SARS)	V_O = 5 V,	T_A = 25°C		0.01	3		0.01	3	μA
		V_O = 0,	T_A = 25°C		−0.01	−3		−0.01	−3	
C_i	Input capacitance				5			5		pF
C_o	Output capacitance				5			5		pF

†All parameters are measured under open-loop conditions with zero common-mode input voltage (unless otherwise specified).
‡All typical values are at V_{CC} = V+ = 5 V, T_A = 25°C

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = V+ = 5 V, f_{clock} = 250 kHz (unless otherwise noted)

analog and converter section

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{ICR}	Common-mode input voltage range		See Note 4	−0.05 to V_{CC}+0.05			V
$I_{I(stdby)}$	Standby input current (see Note 5)	On-channel	V_I = 5 V at on-channel,			1	μA
		Off-channel	V_I = 0 at off-channel			−1	
		On-channel	V_I = 0 at on-channel,			−1	
		Off-channel	V_I = 5 V at off-channel			1	
$r_{i(ref)}$	Input resistance to reference ladder			1.3	2.4	5.9	kΩ

total device

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_Z	Internal zener diode breakdown voltage	I_I = 15 mA at V+ pin, See Note 2	6.3	7	8.5	V
I_{CC}	Supply current			1	2.5	mA

†All parameters are measured under open-loop conditions with zero common-mode input voltage.
‡All typical values are at V_{CC} = 5 V, V+ = 5 V, T_A = 25°C.

NOTES: 2. Internal zener diodes are connected from the V_{CC} input to ground and from the V+ input to ground. The breakdown voltage of each zener diode is approximately 7 V. One zener diode can be used as a shunt regulator and connects to V_{CC} through a regular diode. When the voltage regulator powers the converter, this zener and regular diode combination ensures that the V_{CC} input (6.4 V) is less than the zener breakdown voltage. A series resistor is recommended to limit current into the V+ input.

4. If channel IN− is more positive than channel IN+, the digital output code will be 0000 0000. Connected to each analog input are two on-chip diodes that conduct forward current for analog input voltages one diode drop above V_{CC}. Care must be taken during testing at low V_{CC} levels (4.5 V) because high-level analog input voltage (5 V) can, especially at high temperatures, cause this input diode to conduct and cause errors for analog inputs that are near full-scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V to 5 V input voltage range requires a minimum V_{CC} of 4.950 V for all variations of temperature and load.

5. Standby input currents are currents going into or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state condition.

operating characteristics $V+ = V_{CC} = 5$ V, $f_{clock} = 250$ kHz, $t_r = t_f = 20$ ns, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	BI, BC SUFFIX			AI, AC SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply-voltage variation error		V_{CC} = 4.75 V to 5.25 V		±1/16	±1/4		±1/16	±1/4	LSB
Total unadjusted error (see Note 6)		V_{ref} = 5 V, T_A = MIN to MAX			±1/2			±1	LSB
Common-mode error		Differential mode		±1/16	±1/4		±1/16	±1/4	LSB
Change in zero-error from V_{CC} = 5 V to internal zener diode operation (see Note 2)		I_I = 15 mA at V+ pin, V_{ref} = 5 V, V_{CC} open			1			1	LSB
t_{pd} Propagation delay time, output data after CLK↓ (see Note 7)	MSB-first data	C_L = 100 pF		650	1500		650	1500	ns
	LSB-first data			250	600		250	600	
t_{dis} Output disable time, DO or SARS after CS↑		C_L = 10 pF, R_L = 10 kΩ		125	250		125	250	ns
		C_L = 100 pF, R_L = 2 kΩ			500			500	
t_{conv} Conversion time (multiplexer addressing time not included)					8			8	clock periods

†All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 2. Internal zener diodes are connected from the V_{CC} input to ground and from the V+ input to ground. The breakdown voltage of each zener diode is approximately 7 V. One zener diode can be used as a shunt regulator and connects to V_{CC} through a regular diode. When the voltage regulator powers the converter, this zener and regular diode combination ensures that the V_{CC} input (6.4 V) is less than the zener breakdown voltage. A series resistor is recommended to limit current into the V+ input.

6. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.
7. The most significant bit (MSB) data is output directly from the comparator and therefore requires additional delay to allow for comparator response time.

PARAMETER MEASUREMENT INFORMATION

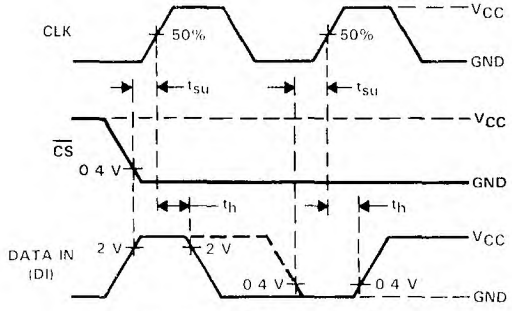


FIGURE 1. DATA INPUT TIMING

PARAMETER MEASUREMENT INFORMATION

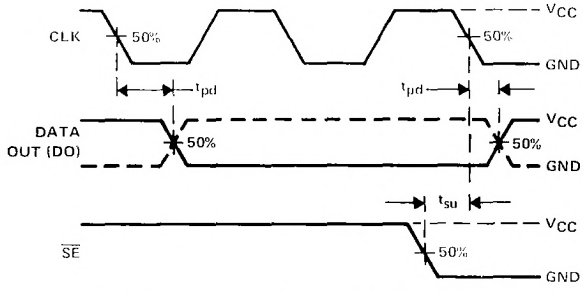
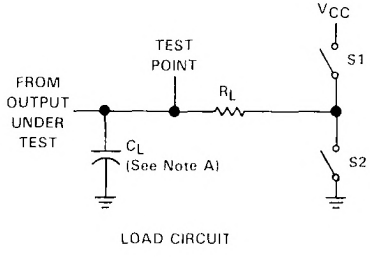
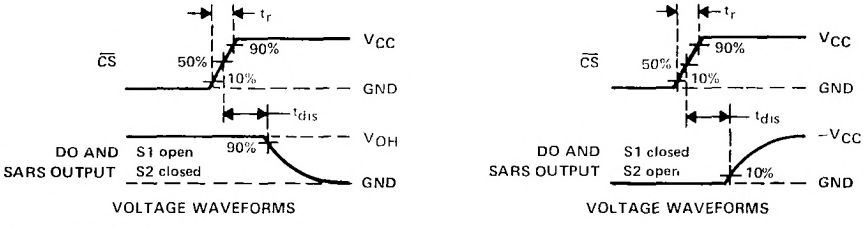


FIGURE 2. DATA OUTPUT TIMING



LOAD CIRCUIT



NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. OUTPUT DISABLE TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

UNADJUSTED OFFSET ERROR
vs
REFERENCE VOLTAGE

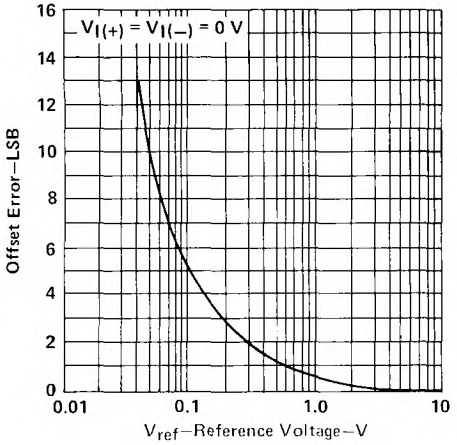


FIGURE 4

LINEARITY ERROR
vs
REFERENCE VOLTAGE

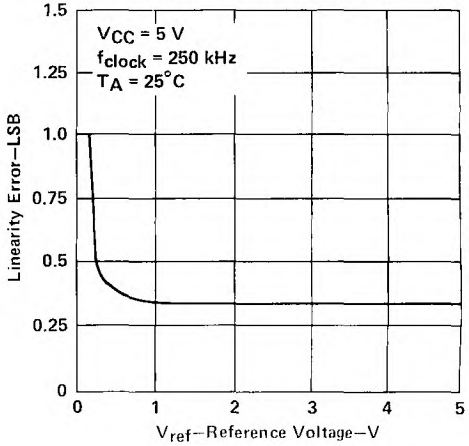


FIGURE 5

LINEARITY ERROR
vs
FREE-AIR TEMPERATURE

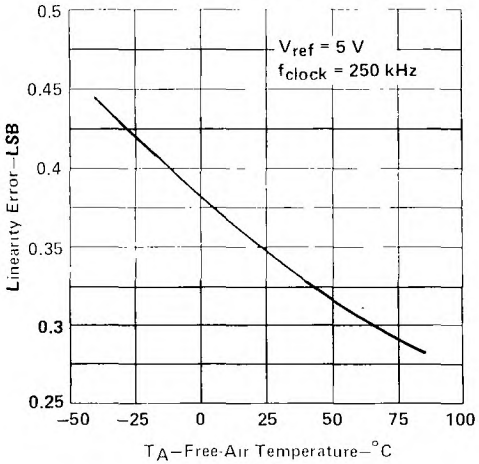


FIGURE 6

LINEARITY ERROR
vs
CLOCK FREQUENCY

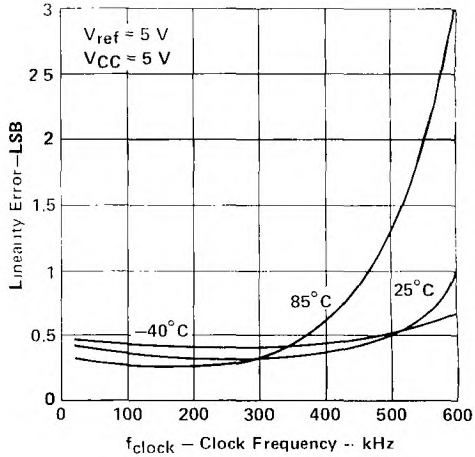


FIGURE 7

TYPICAL CHARACTERISTICS

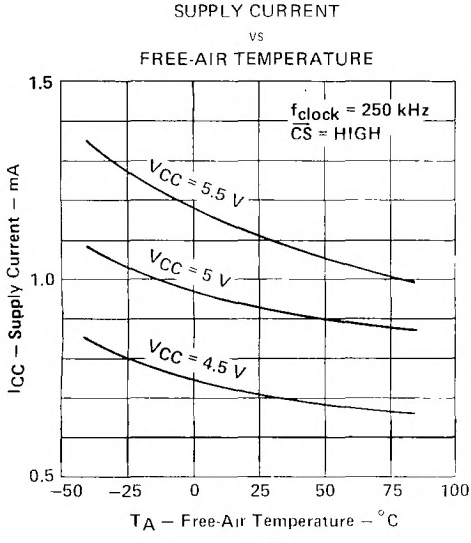


FIGURE 8

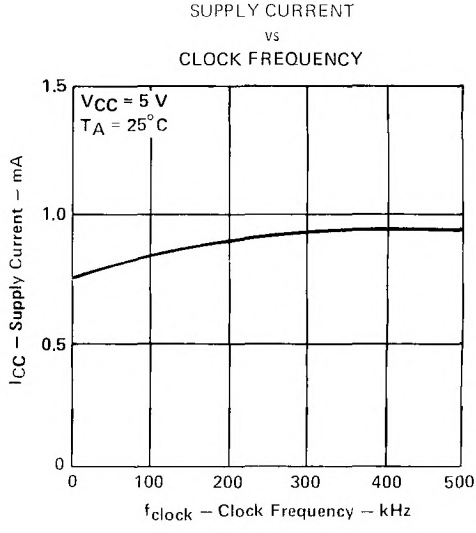


FIGURE 9

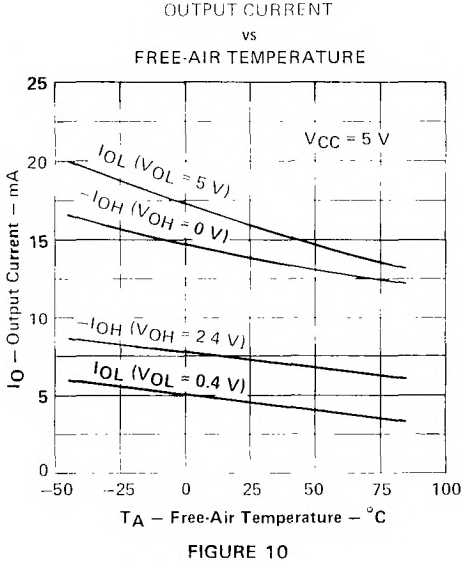
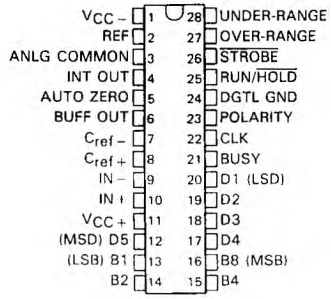


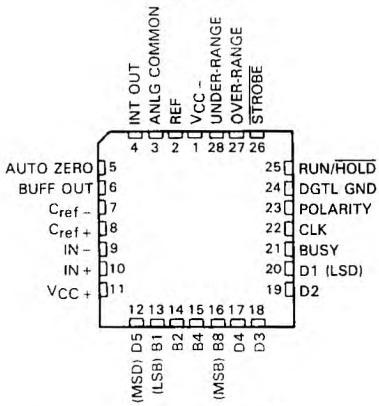
FIGURE 10

- Advanced LinCMOS™ Technology
- Zero Reading for 0-V Input
- Precision Null Detection with True Polarity at Zero
- 1-pA Typical Input Current
- True Differential Input
- Multiplexed Binary-Coded-Decimal Output
- Low Rollover Error: ±1 Count Maximum
- Control Signals Allow Interfacing with UARTs or Microprocessors
- Autoranging Capability with Over- and Under-Range Signals
- TTL-Compatible Outputs
- Direct Replacement for Teledyne TSC7135, Intersil ICL7135, Maxim ICL7135, and Siliconix Si7135

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The ICL7135C and TLC7135C converters are manufactured with Texas Instruments highly efficient Advanced LinCMOS™ technology. This 4 1/2-digit dual-slope-integrating analog-to-digital converter is designed to provide interfaces to both a microprocessor and a visual display. The digit-drive outputs D1 through D4 and multiplexed binary-coded-decimal outputs, B1 through B4, provide an interface for LED or LCD decoder/drivers as well as microprocessors.

The ICL7135C and TLC7135C offer 50-ppm (one part in 20,000) resolution with a maximum linearity error of one count. The zero error is less than 10 μV and zero drift is less than 0.5 μV/°C. Source-impedance errors are minimized by low input current (less than 10 pA). Rollover error is limited to ±1 count.

The BUSY, $\overline{\text{STROBE}}$, RUN/$\overline{\text{HOLD}}$, OVER-RANGE, and UNDER-RANGE control signals support microprocessor-based measurement systems. The control signals also can support remote data acquisition systems with data transfer via universal asynchronous receiver transmitters (UARTs).

The ICL7135C and TLC7135C are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS†

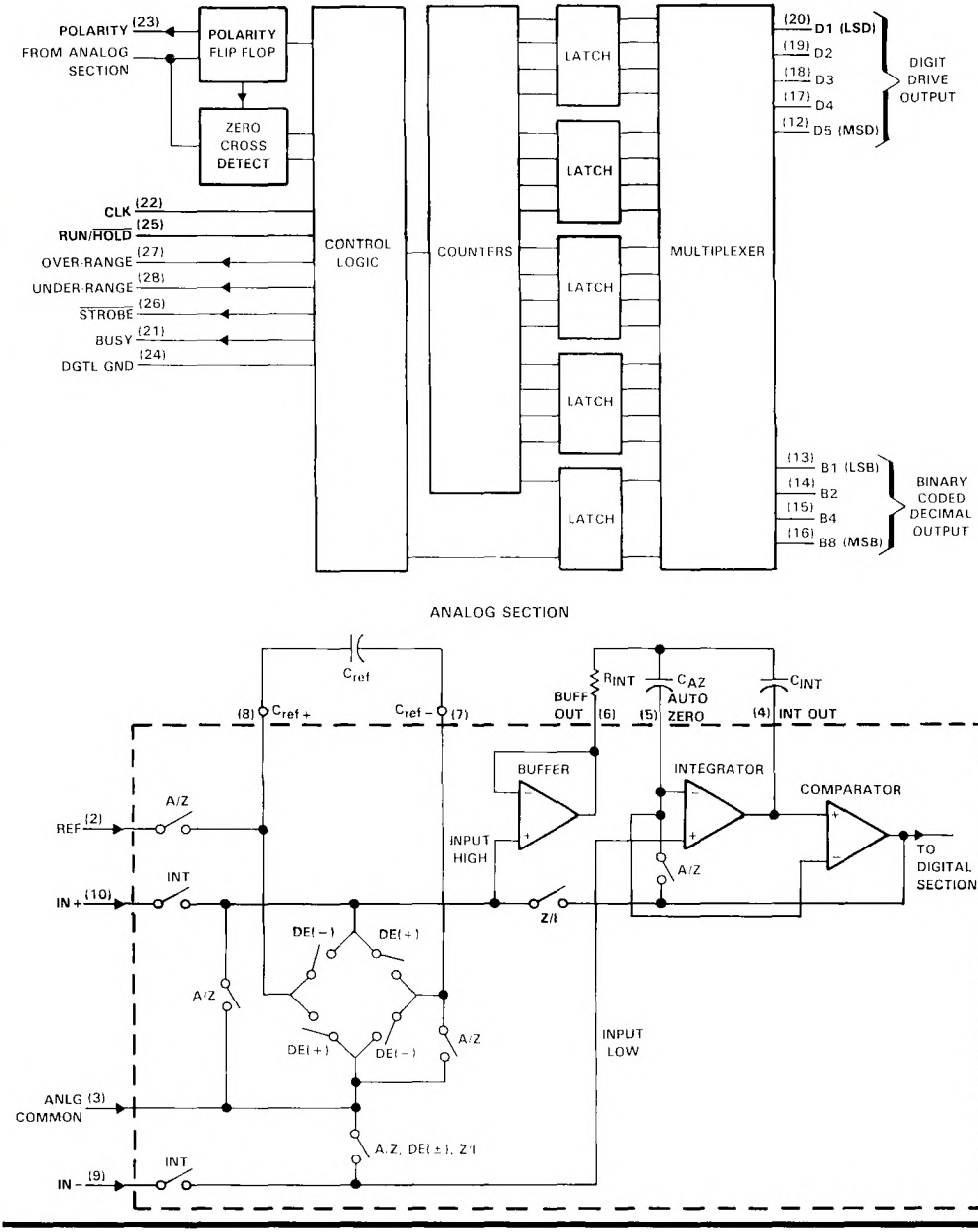
SYMBOLIZATION		OPERATING
DEVICE	PACKAGE SUFFIX	TEMPERATURE RANGE
ICL7135C	FN, N	0°C to 70°C
TLC7135C	FN, N	0°C to 70°C

† In many instances, these ICs may have ICL7135C and TLC7135C symbolization on the package.

Caution. This device has limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage.

Advanced LinCMOS™ *is a trademark* of Texas Instruments Incorporated.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (V_{CC+} with respect to V_{CC-}) . . . . . 15 V
Analog input voltage (pin 9 or pin 10) . . . . . V_{CC-} to V_{CC+}
Reference voltage range . . . . . V_{CC-} to V_{CC+}
Clock input voltage range . . . . . 0 V to V_{CC+}
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Case temperature for 10 seconds: FN package . . . . . 260°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4	5	6	V
Supply voltage, V_{CC-}	−3	−5	−8	V
Reference voltage, V_{ref}		1		V
High-level input voltage, CLK, RUN/$\overline{HOLD}$, V_{IH}	2.8			V
·· level input voltage, CLK, RUN/$\overline{HOLD}$, V_{IL}			0.8	V
·ential input voltage, V_{ID}	V_{CC-} +1		V_{CC+} −0.5	V
Maximum operating frequency, f_{clock} (see Note 1)	1.2	2		MHz
Operating free-air temperature range, T_A	0		70	°C

NOTE 1. Clock frequency range extends down to 0 Hz

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{ref} = 1 V, f_{clock} = 120 kHz, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	D1-D5,B1,B2,B4,B8	I_O = −1 mA		2.4		5	V
		Other outputs	I_O = −10 μA		4.9		5	
V_{OL}	Low-level output voltage		I_O = 1.6 mA				0.4	V
	Peak-to-peak output noise voltage (see Note 2)		V_{ID} = 0,	Full Scale = 2 V		15		μV
α_{VO}	Zero-reading temperature coefficient of output voltage		V_{ID} = 0,	0°C ≤ T_A ≤ 70°C		0.5	2	μV/°C
I_{IH}	High-level input current		V_I = 5 V,	0°C ≤ T_A ≤ 70°C		0.1	10	μA
I_{IL}	Low-level input current		V_I = 0 V,	0°C ≤ T_A ≤ 70°C		−0.02	−0.1	mA
I_I	Input leakage current, pins 9 and 10		V_{ID} = 0	T_A = 25°C		1	10	pA
				0°C ≤ T_A ≤ 70°C			250	
I_{CC+}	Positive supply current		f_{clock} = 0	T_A = 25°C		1	2	mA
				0°C ≤ T_A ≤ 70°C			3	
I_{CC-}	Negative supply current		f_{clock} = 0	T_A = 25°C		−0.8	−2	mA
				0°C ≤ T_A ≤ 70°C			−3	
C_{pd}	Power dissipation capacitance		See Note 3			40		pF

NOTES: 2. This is the peak-to-peak value that is not exceeded 95% of the time.
3. Factor relating clock-frequency to increase in supply current. At V_{CC+} = 5 V

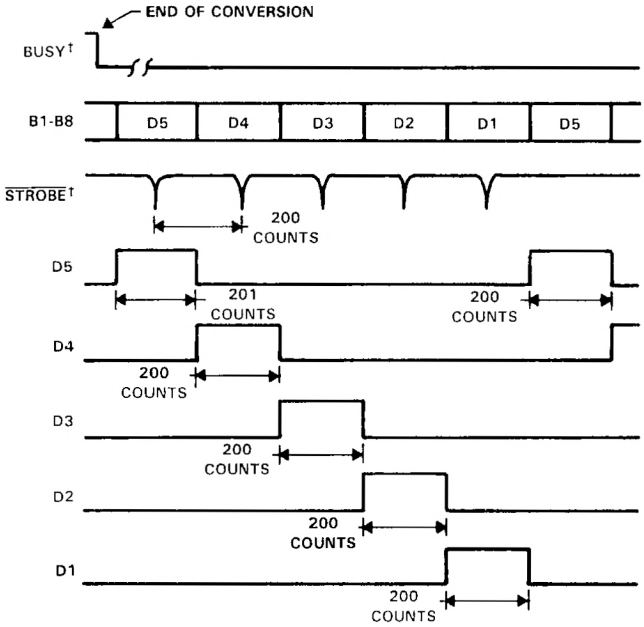
$$I_{CC+} = I_{CC+}(f_{clock} = 0) + C_{pd} \times 5\ V \times f_{clock}$$

operating characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{ref} = 1 V, f_{clock} = 120 kHz, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
α_{FS}	Full-scale temperature coefficient (see Note 4)	V_{ID} = 2 V, 0°C ≤ T_A ≤ 70°C			5	ppm/°C
	Linearity error	−2 V ≤ V_{ID} ≤ 2 V		0.5	1	count
	Differential linearity error (see Note 5)	−2 V ≤ V_{ID} ≤ 2 V		0.01		LSB
	± Full-scale symmetry error (see Note 6) (rollover error)	V_{ID} = ±2 V		0.5	1	count
	Display reading with 0-V input	V_{ID} = 0, 0°C ≤ T_A ≤ 70°C	−0.0000	±0.0000	+0.0000	Digital Reading
	Display reading in ratiometric operation	V_{ID} = V_{ref}, T_A = 25°C	+0	+0	+1	Digital Reading
		0°C ≤ T_A ≤ 70°C	+0	+0	+1	

NOTES: 4. This parameter is measured with an external reference having a temperature coefficient of less than 0.01 ppm/°C.
5. The magnitude of the difference between the worst case step of adjacent counts and the ideal step.
6. Rollover error is the difference between the absolute values of the conversion for 2 V and −2 V.

timing diagrams



† Delay between BUSY going low and the first STROBE pulse is dependent upon the analog input.

FIGURE 1

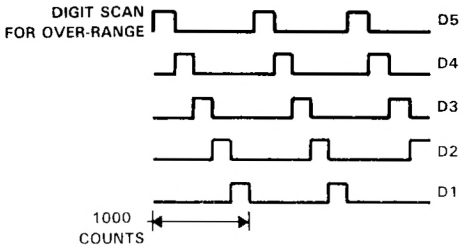


FIGURE 2

timing diagrams (continued)

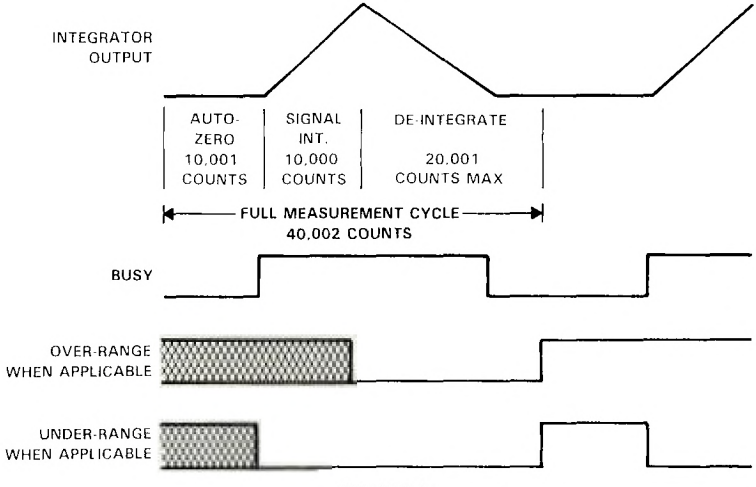
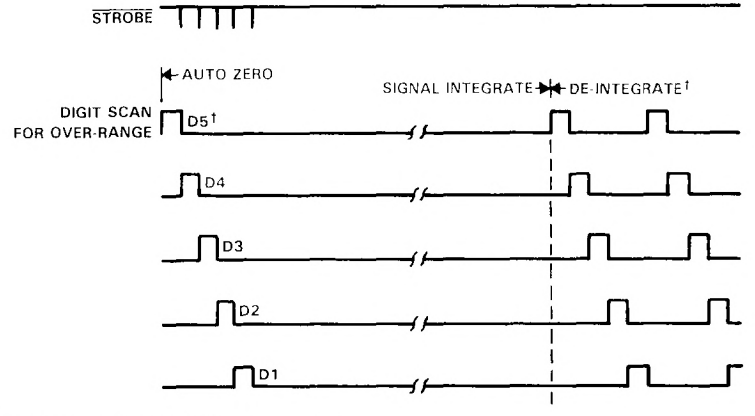


FIGURE 3



†First D5 of AUTO ZERO and DE-INTEGRATE is one count longer

FIGURE 4

PRINCIPLES OF OPERATION

A measurement cycle for the ICL7135C and TLC7135C consists of the following four phases.

1. Auto-Zero Phase. The internal IN+ and IN− inputs are disconnected from the pins and internally connected to ANLG COMMON. The reference capacitor is charged to the reference voltage. The system is configured in a closed loop and the auto-zero capacitor is charged to compensate for offset voltages in the buffer amplifier, integrator, and comparator. The auto-zero accuracy is limited only by the system noise, and the overall offset, as referred to the input, is less than 10 μV.
2. Signal Integrate Phase. The auto-zero loop is opened and the internal IN+ and IN− inputs are connected to the external pins. The differential voltage between these inputs is integrated for a fixed period of time. If the input signal has no return with respect to the converter power supply, IN− can be tied to ANLG COMMON to establish the correct common-mode voltage. Upon completion of this phase, the polarity of the input signal is recorded.
3. De-integrate Phase. The reference is used to perform the de-integrate task. The internal IN− is internally connected to ANLG COMMON and IN+ is connected across the previously charged reference capacitor. The recorded polarity of the input signal is used to ensure that the capacitor will be connected with the correct polarity so that the integrator output polarity will return to zero. The time, which is required for the output to return to zero, is proportional to the amplitude of the input signal. The return time is displayed as a digital reading and is determined by the equation 10,000 x (V_{ID}/V_{ref}). The maximum or full-scale conversion occurs when V_{ID} is two times V_{ref}.
4. Zero Integrator Phase. The internal IN− is connected to ANLG COMMON. The system is configured in a closed loop to cause the integrator output to return to zero. Typically this phase requires 100 to 200 clock pulses. However, after an over-range conversion, 6200 pulses are required.

description of analog circuits

input signal range

The common mode range of the input amplifier extends from 1 V above the negative supply to 1 V below the positive supply. Within this range, the common mode rejection ratio (CMRR) is typically 86 dB. Both differential and common mode voltages cause the integrator output to swing. Therefore, care must be exercised to assure the integrator output does not saturate.

analog common

Analog common (ANLG COMMON) is connected to the internal IN− during the auto-zero, de-integrate, and zero integrator phases. If IN− is connected to a voltage which is different than analog common during the signal integrate phase, the resulting common mode voltage will be rejected by the amplifier. However, in most applications, IN LO will be set at a known fixed voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common mode voltage from the converter. Removing the common mode voltage in this manner will slightly increase conversion accuracy.

reference

The reference voltage is positive with respect to analog common. The accuracy of the conversion result is dependent upon the quality of the reference. Therefore, to obtain a high accuracy conversion, a high quality reference should be used.

description of digital circuits

RUN/$\overline{\text{HOLD}}$ input

When the RUN/$\overline{\text{HOLD}}$ input is high or open, the device will continuously perform measurement cycles every 40,002 clock pulses. If this input is taken low, the IC will continue to perform the ongoing measurement cycle and then hold the conversion reading for as long as the pin is held low. If the pin is held low after completion of a measurement cycle, a short positive pulse (greater than 300 ns) will initiate a new measurement cycle. If this positive pulse occurs before the completion of a measurement cycle, it will not be recognized. The first STROBE pulse, which occurs 101 counts after the end of a measurement cycle, is an indication of the completion of a measurement cycle. Thus, the positive pulse could be used to trigger the start of a new measurment after the first STROBE pulse.

$\overline{\text{STROBE}}$ input

Negative going pulses from this input are used to transfer the BCD conversion data to external latches, UARTS, or microprocesors. At the end of the measurement cycle, the digit-drive (D5) input goes high and remains high for 201 counts. The most significant digit (MSD) BCD bits are placed on the BCD pins. After the first 101 counts, halfway through the duration of output D1-D5 going high, the $\overline{\text{STROBE}}$ pin goes low for 1/2 clock pulse width. The placement of the $\overline{\text{STROBE}}$ pulse at the midpoint of the D5 high pulse allows the information to be latched into an external device on either a low-level or an edge. Such placement of the $\overline{\text{STROBE}}$ pulse also ensures that the BCD bits for the second MSD will not yet be competing for the BCD lines and latching of the correct bits is assured. The above process is repeated for the second MSD and the D4 output. Similarly, the process is repeated through the least significant digit (LSD). Subsequently, inputs D5 through D1 and the BCD lines will continue scanning without the inclusion of $\overline{\text{STROBE}}$ pulses. This subsequent continuous scanning causes the conversion results to be continuously displayed. Such subsequent scanning does not occur when an over-range condition occurs.

BUSY output

The BUSY output goes high at the beginning of the signal integrate phase and remains high until the first clock pulse after zero-crossing or at the end of the measurement cycle if an over-range condition occurs. It is possible to use the BUSY pin to serially transmit the conversion result. Serial transmission can be accomplished by ANDing the BUSY and CLOCK signals and transmitting the ANDed output. The transmitted output consists of 10,001 clock pulses, which occur during the signal integrate phase, and the number of clock pulses, which occur during the de-integrate phase. The conversion result can be obtained by subtracting 10,001 from the total number of clock pulses.

OVER-RANGE output

When an over-range condition occurs, this pin goes high after the BUSY signal goes low at the end of the measurement cycle. As previously noted, the BUSY signal remains high until the end of the measurement cycle when an over-range condition occurs. The OVER-RANGE output goes high at end of BUSY and goes low at the beginning of the de-integrate phase in the next measurement cycle.

UNDER-RANGE output

At the end of the BUSY signal, this pin goes high if the conversion result is less than or equal to 9% (count of 1800) of the full-scale range. The UNDER-RANGE output is brought low at the beginning of the signal integrate phase of the next measurement cycle.

PRINCIPLES OF OPERATION

POLARITY output

The POLARITY output is high for a positive input signal and is updated at the beginning of each de-integrate phase. The polarity output is valid for all inputs including ±0 and over-range signals.

digit-drive (D5, D4, D2 and D1) outputs

Each digit-drive output (D1 through D5) sequentially goes high for 200 clock pulses. This sequential process is continuous unless an over-range occurs. When an over-range occurs, all of the digit drive outputs are blanked from the end of the strobe sequence until the beginning of the de-integrate phase (when the sequential digit drive activation begins again). The blanking activity, during an over-range condition, may be used to cause the display to flash and indicate the over-range condition.

BCD outputs

The BCD bits (B8, B4, B2 and B1) for a given digit are sequentially activated on these outputs. Simultaneously, the appropriate Digit-drive line for the given digit is activated.

system aspects

integrating resistor

The value of the integrating resistor (R_{INT}) is determined by the full scale input voltage and the output current of the integrating amplifier. The integrating amplifier can supply 20 μA of current with negligible non-linearity. The equation for determining the value of this resistor is as follows:

$$R_{INT} = \frac{\text{FULL-SCALE VOLTAGE}}{I_{INT}}$$

Integrating amplifier current, I_{INT}, from 5 to 40 μA will yield good results. However, the nominal and recommended current is 20 μA.

integrating capacitor

The product of the integrating resistor and capacitor should be selected to give the maximum voltage swing without causing the integrating amplifier output to saturate and get too close to the power supply voltages. If the amplifier output is within 0.3 V of either supply, saturation will occur. With ±5-V supplies and ANLG COMMON connected to ground, the designer should design for a ±3.5-V to ±4-V integrating amplifier swing. A nominal capacitor value is 0.47 μF. The equation for determining the value of the integrating capacitor (C_{INT}) is as follows:

$$C_{INT} = \frac{10{,}000 \times \text{CLOCK PERIOD} \times I_{INT}}{\text{INTEGRATOR OUTPUT VOLTAGE SWING}}$$

where: I_{INT} is nominally 20 μA.

Capacitors with large tolerances and high dielectric absorption can induce conversion inaccuracies. A capacitor, which is too small could cause the integrating amplifier to saturate. High dielectric absorption causes the effective capacitor value to be different during the signal integrate and de-integrate phases. Polypropylene capacitors have very low dielectric absorption. Polystyrene and Polycarbonate capacitors have higher dielectric absorption, but also work well.

PRINCIPLES OF OPERATION

auto-zero and reference capacitor

Large capacitors will tend to reduce noise in the system. Dielectric absorption is unimportant except during power-up or overload recovery. Typical values are 1 μF.

reference voltage

For high-accuracy absolute measurements, a high quality reference should be used.

rollover resistor and diode

The ICL7135C and TLC7135C have a small rollover error, however it can be corrected. The correction is to connect the cathode of any silicon diode to the INT OUT pin and the anode to a resistor. The other end of the resistor is connected to ANLG COMMON or ground. For the recommended operating conditions the resistor value is 100 kΩ. This value may be changed to correct any rollover error which has not been corrected. In many non-critical applications, the resistor and diode are not needed.

maximum clock frequency

For most dual-slope A/D converters, the maximum conversion rate is limited by the frequency response of the comparator. In this circuit, the comparator follows the integrator ramp with a 3 μs delay. Therefore, with a 160-kHz clock frequency (6 μs period), half of the first reference integrate clock period is lost in delay. Hence, the meter reading will change from 0 to 1 with a 50-μV input, 1 to 2 with a 150-μV input, 2 to 3 with a 250-μV input, etc. This transition at midpoint is desirable; however, if the clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted. The above transition points assume a 2-V input range is equivalent to 20,000 clock cycles.

If the input signal is always of one polarity, comparator delay need not be a limitation. Clock rates of 1 MHz are possible since non-linearity and noise do not increase substantially with frequency. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

For signals with both polarities, the clock frequency can be extended above 160 kHz without error by using a low value resistor in series with the integrating capacitor. This resistor causes the integrator to jump slightly towards the zero-crossing level at the beginning of the de-integrate phase and thus, compensates for the comparator delay. This series resistor should be 10 Ω to 50 Ω. This approach allows clock frequencies up to 480 kHz.

minimum clock frequency

The minimum clock frequency limitations result from capacitor leakage from the auto-zero and reference capacitors. Measurement cycles as high as 10 s are not influenced by leakage error.

rejection of 50 Hz or 60 Hz pickup

To maximize the rejection of 50 Hz or 60 Hz pickup, the clock frequency should be chosen so that an integral multiple of 50 Hz or 60 Hz periods occur during the signal integrate phase. To achieve rejection of these signals, some clock frequencies which could be used are as follows:

50 Hz: 250, 166.66, 125, 100 kHz, etc.
60 Hz: 300, 200, 150, 120, 100, 40, 33.33 kHz, etc.

PRINCIPLES OF OPERATION

zero-crossing flip-flop

This flip-flop interrogates the comparator's zero-crossing status. The interrogation is performed after the previous clock cycle and the positive half of the ongoing clock cycle have occurred so that any comparator transients which result from the clock pulses do not affect the detection of a zero-crossing. This procedure delays the zero-crossing detection by one clock cycle. To eliminate the inaccuracy, which is caused by this delay, the counter is disabled for one clock cycle at the beginning of the de-integrate phase. Therefore, when the zero-crossing is detected one clock cycle later than the zero-crossing actually occurs, the correct number of counts is displayed.

noise

The peak-to-peak noise around zero is approximately 15 μV (peak-to-peak value not exceeded 95% of the time). Near full scale, this value increases to approximately 30 μV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

analog and digital grounds

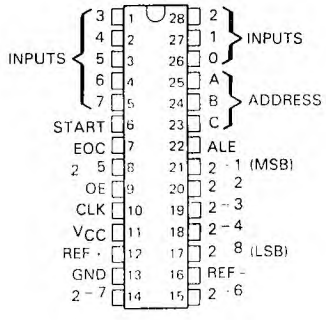
For high-accuracy applications, ground loops must be avoided. Return currents from digital circuits must not be sent to the analog ground line.

power supplies

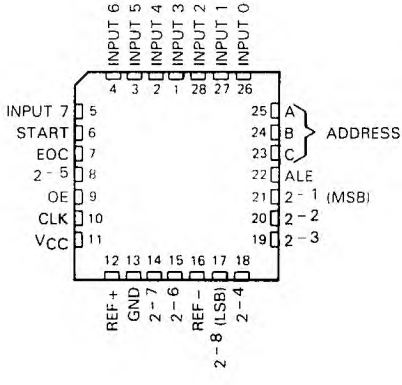
The ICL7135C and TLC7135C are designed to work with ±5-V power supplies. However, 5-V operation is possible if the input signal does not vary more than ±1.5 V from mid-supply.

- Total Unadjusted Error . . . ±0.75 LSB Max for TL0808 and ±1.25 LSB Max for TL0809 Over Temperature Range
- Ideal for Battery Operated, Portable Instrumentation Applications
- Resolution of 8 Bits
- 100 μs Conversion Time
- Ratiometric Conversion
- Monotonic Over the Entire A/D Conversion Range
- No Missing Codes
- Easy Interface with Microprocessors
- Latched 3-State Outputs
- Latched Address Inputs
- Single 2.75-V to 5.5-V Supply
- Extremely Low Power Consumption . . . 0.3 mW Typ
- Improved Direct Replacements for ADC0808, ADC0809

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



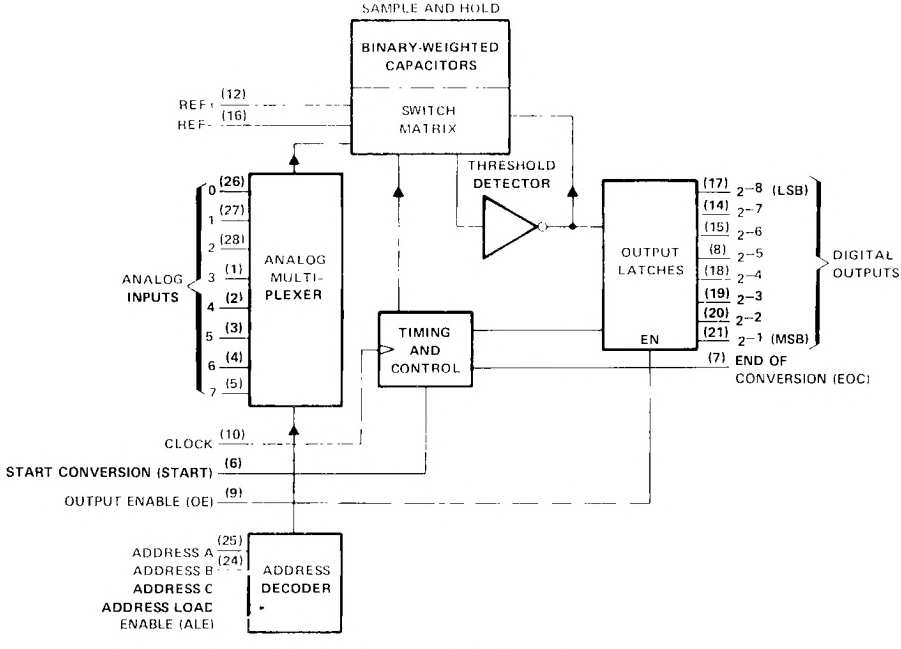
description

The TL0808 and TL0809 are monolithic CMOS devices with an 8-channel multiplexer, an 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to the comparator. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a switched-capacitor array, a sample-and-hold, and a successive-approximation register (SAR). Detailed information on interfacing to most popular microprocessors is readily available from the factory. These devices are designed to operate from common microprocessor control buses, with three-state output latches driving the data bus. The devices can be made to appear to the microprocessor as a memory location or an I/O port.

The comparison and converting methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs from the SAR and latched inputs to the multiplexer address decoder. The single 2.75-V to 5.5-V supply and extremely low power requirements make the TL0808 and TL0809 especially useful for a wide variety of applications including portable battery and LCD applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

The TL0808 and TL0809 are characterized for operation from −40°C to 85°C.

functional block diagram (positive logic)



MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low to high transition

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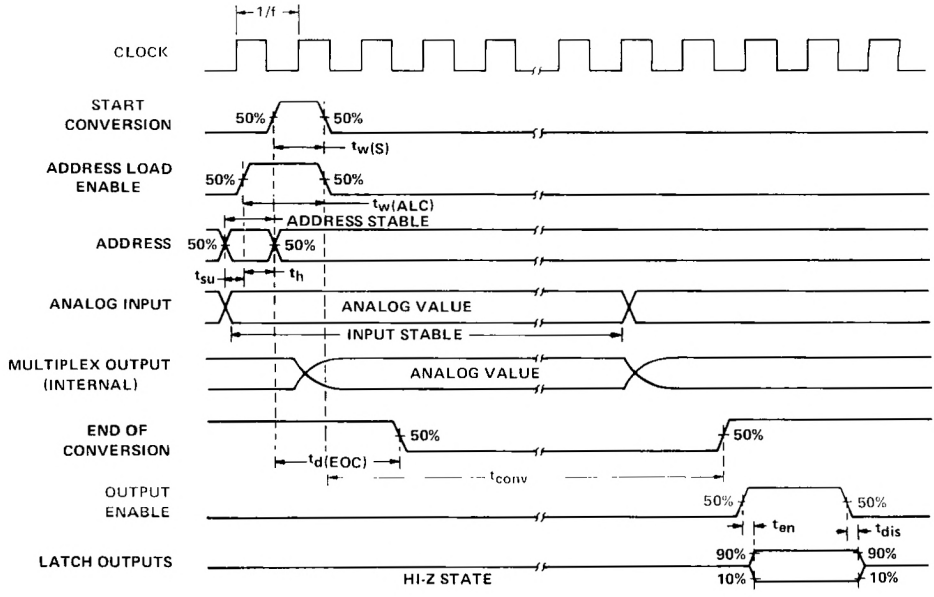
operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: control inputs . . . . . −0.3 to 15 V
all other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	2.75		5.5	V
Positive reference voltage, V_{ref+} (see Notes 2, 3, and 4)	2.75	V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{ref-} (see Notes 2, 3, and 4)	−0.1	0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 4)		3		V
High-level input voltage, control inputs, V_{IH}	0.7 V_{CC}			V
Low-level input voltage, control inputs, V_{IL}			0.3 V_{CC}	V
Operating free-air temperature, T_A (see Note 4)	−40		85	°C

NOTES: 2. The accuracy of the conversion will depend on the stability of the reference voltages applied.
3. Analog voltages greater than or equal to V_{ref+} convert to all highs, and all voltages less than V_{ref-} convert to all lows.
4. For proper operation of the TL0808 and TL0809 at free-air temperatures below 0°C, V_{CC} and ($V_{ref+} - V_{ref-}$) should not be less than 3 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3 V to 5.25 V (unless otherwise noted)

total device

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_O = −360 μA	V_{CC}−0.6			V
V_{OL}	Low-level output voltage	Data outputs	I_O = 1.6 mA			0.45	V
		End of conversion	I_O = 1.2 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current		V_O = V_{CC}			1	μA
			V_O = 0			−1	
I_I	Control input current at maximum input voltage		V_I = 15 V			1	μA
I_{IL}	Low-level control input current		V_I = 0			−1	μA
I_{CC}	Supply current		V_{CC} = 3 V, f_{clock} = 640 kHz		100	500	μA
			V_{CC} = 5 V, f_{clock} = 640 kHz		0.3	3	mA
C_i	Input capacitance, control inputs		T_A = 25°C		10	15	pF
C_o	Output capacitance, data outputs		T_A = 25°C		10	15	pF
	Resistance from pin 12 to pin 16			1	1000		kΩ

†Typical values are at V_{CC} = 3 V and T_A = 25°C.

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analog multiplexer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{on}	Channel on-state current (see Note 5)	V_I = 3 V,	f_{clock} = 640 kHz			2	μA
		V_I = 0,	f_{clock} = 640 kHz			−2	
I_{off}	Channel off-state current	V_{CC} = 3 V, T_A = 25°C	V_I = 3 V		10	200	nA
			V_I = 0		−10	−200	
		V_{CC} = 3 V	V_I = 3 V			1	μA
			V_I = 0			−1	

†Typical values are at V_{CC} = 3 V and T_A = 25°C.

NOTE 5: Channel on-state current is primarily due to the bias current into or out of the threshold detector, and it varies directly with clock frequency

timing requirements, T_A = 25°C, V_{CC} = V_{ref+} = 3 V, V_{ref-} = 0 (unless otherwise noted)

			MIN	TYP†	MAX	UNIT
t_{conv}	Conversion time (see Note 6)		90		116	μs
f_{clock}	Clock frequency	V_{CC} = 2.75 V to 4 V	10		640	kHz
		V_{CC} = 4 V to 5.5 V	10		1280	
$t_{w(s)}$	Start pulse duration		200			ns
$t_{w(ALC)}$	Address load control pulse duration		200			ns
t_{su}	Address setup time		50			ns
t_h	Address hold time		50			ns
$t_{d(EOC)}$	Delay time, end of conversion output (see Notes 6 and 7)		0		14.5	μs

operating characteristics, T_A = 25°C, V_{CC} = V_{ref+} = 3 V, V_{ref-} = 0, f_{clock} = 640 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TL0808			TL0809			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
k_{SVS}	Supply voltage sensitivity	V_{CC} = V_{ref+} = 3 V to 5.25 V, T_A = −40°C to 85°C, See Note 8			±0.05			±0.05		%/V
	Linearity error (see Note 9)				±0.5			±1		LSB
	Zero error (see Note 10)				±0.5			±0.5		LSB
	Total unadjusted error (See Note 11)	f_{clock} = 125 kHz	T_A = 25°C		±0.25	±0.5		±0.5	±1	LSB
			T_A = −40°C to 85°C			±0.75			±1.25	
t_{en}	Output enable time	C_L = 50 pF, R_L = 10 kΩ			80	250		80	250	ns
t_{dis}	Output disable time	C_L = 10 pF, R_L = 10 kΩ			105	300		105	300	ns

†Typical values for all except supply voltage sensitivity are at V_{CC} = 3 V.

NOTES: 6. Refer to the operating sequence diagram.

7. For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock periods plus 2 μs.
8. Supply voltage sensitivity relates to the ability of an analog-to-digital converter to maintain accuracy as the supply voltage varies. The supply and V_{ref+} are varied together and the change in accuracy is measured with respect to full-scale.
9. Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.
10. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
11. Total unadjusted error is the maximum sum of linearity error, zero error, and full-scale error.

PRINCIPLES OF OPERATION

The TL0808 and TL0809 each consists of an analog signal multiplexer, an 8-bit successive-approximation converter, and related control and output circuitry.

multiplexer

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the address decoder. Address load control loads the address code into the decoder on a low-to-high transition. The output latch is reset by the positive-going edge of the start pulse. Sampling also starts with the positive-going edge of the start pulse and lasts for 32 clock periods. The conversion process may be interrupted by a new start pulse before the end of 64 clock periods. The previous data will be lost if a new start of conversion occurs before the 64th clock pulse. Continuous conversion may be accomplished by connecting the End-of-Conversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 1). In the first phase of the conversion process, the analog input is sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 of this capacitor is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF−. If the voltage at the summing node is greater than the trip-point of the threshold detector (approximately one-half the V_{CC} voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF−. If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF+ through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are counted.

With each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is successive approximation, but relies on charge redistribution rather than a successive-approximation register (and reference DAC) to count and weigh the bits from MSB to LSB.

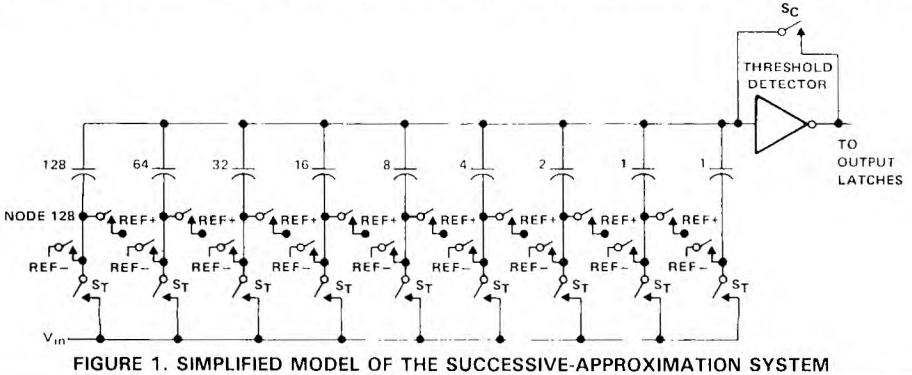

FIGURE 1. SIMPLIFIED MODEL OF THE SUCCESSIVE-APPROXIMATION SYSTEM

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D2234, JUNE 1976 - REVISED SEPTEMBER 1986

- Functionally Interchangeable with Siliconix DG182, DG185, DG188, DG191 with Same Terminal Assignments
- Monolithic Construction
- Adjustable Reference Voltage
- JFET Inputs
- Uniform On-State Resistance for Minimum Signal Distortion
- ±10-V Analog Voltage Range
- TTL, MOS, and CMOS Logic Control Compatibility

description

The TL182, TL185, TL188, and TL191 are monolithic high-speed analog switches using BI-MOS technology. They comprise JFET-input buffers, level translators, and output JFET switches. The TL182 switches are SPST; the TL185 switches are SPDT. The TL188 is a pair of complementary SPST switches as is each half of the TL191.

A high level at a control input of the TL182 turns the associated switch off. A high level at a control input of the TL185 turns the associated switch on. For the TL188, a high level at the control input turns the associated switches S1 on and S2 off.

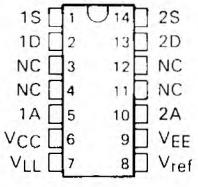
The threshold of the input buffer is determined by the voltage applied to the reference input (V_{ref}). The input threshold is related to the reference input by the equation $V_{th} = V_{ref} + 1.4$ V. Thus, for TTL compatibility, the V_{ref} input is connected to ground. The JFET input makes the device compatible with bipolar, MOD, and CMOS logic families. Threshold compatibility may, again, be determined by $V_{th} = V_{ref} + 1.4$ V.

The output switches are junction field-effect transistors featuring low on-state resistance and high off-state resistance. The monolithic structure ensures uniform matching.

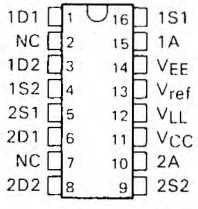
BI-MOS technology is a major breakthrough in linear integrated circuit processing. BI-MOS can have ion-implanted JFETs, p-channel MOS-FETs, plus the usual bipolar components all on the same chip. BI-MOS provides for monolithic circuit designs that previously have been available only as expensive hybrids.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −25°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

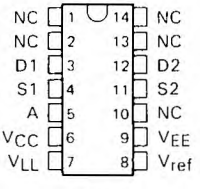
TL182
N PACKAGE
(TOP VIEW)



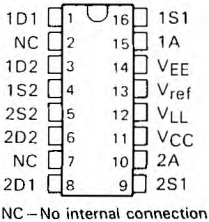
TL185
N PACKAGE
(TOP VIEW)



TL188
N PACKAGE
(TOP VIEW)



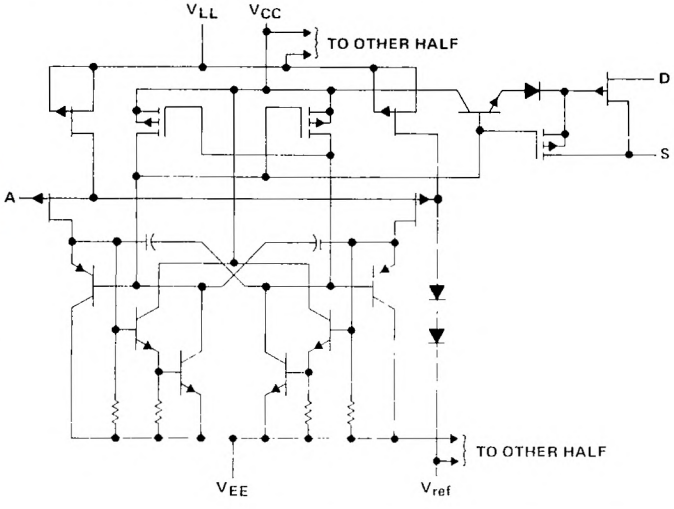
TL191
N PACKAGE
(TOP VIEW)



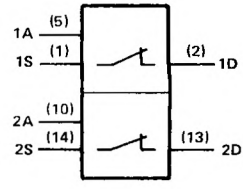
NC—No internal connection

TL182 TWIN SPST SWITCH

schematic (each channel)



symbol

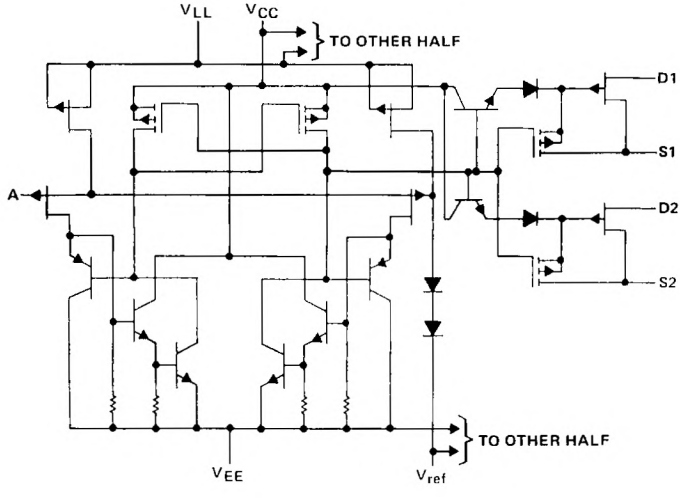


FUNCTION TABLE
(EACH HALF)

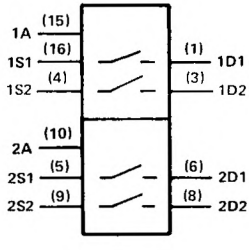
INPUT A	SWITCH S
L	ON (CLOSED)
H	OFF (OPEN)

TL185 TWIN DPST SWITCH

schematic (each channel)



symbol



FUNCTION TABLE
(EACH HALF)

INPUT A	SWITCHES SW1 AND SW2
L	OFF (OPEN)
H	ON (CLOSED)

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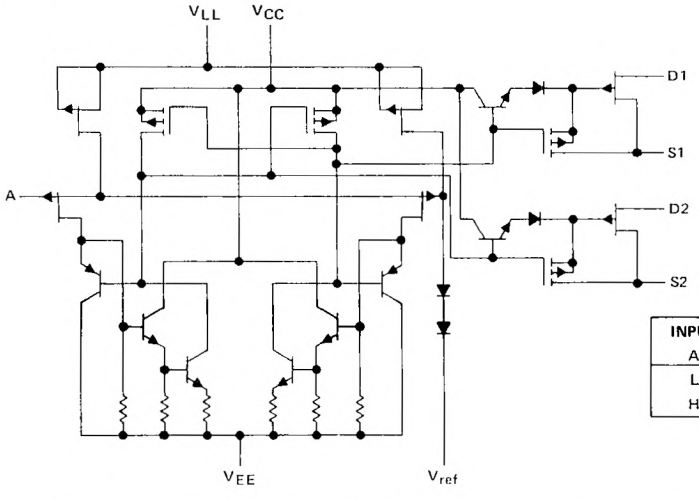
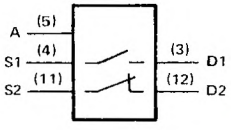
TL188 DUAL COMPLEMENTARY SPST SWITCH

schematic



symbol

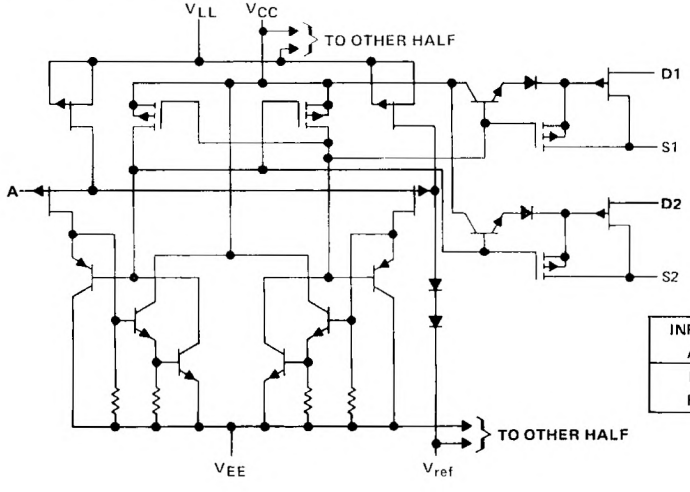


FUNCTION TABLE

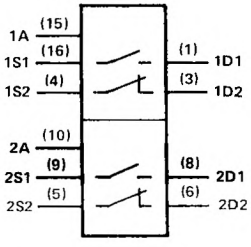
INPUT	SWITCHES	
A	SW1	SW2
L	OFF (OPEN)	ON (CLOSED)
H	ON (CLOSED)	OFF (OPEN)

TL191 TWIN DUAL COMPLEMENTARY SPST SWITCH

schematic (each channel)



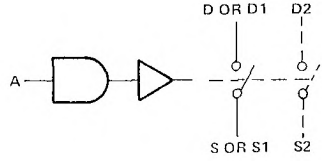
symbol



FUNCTION TABLE

INPUT	SWITCHES	
A	SW1	SW2
L	OFF (OPEN)	ON (CLOSED)
H	ON (CLOSED)	OFF (OPEN)

functional block diagram



See the preceding two pages for operation of the switches.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply to negative supply voltage, $V_{CC} - V_{EE}$ . . . . . 36 V
Positive supply voltage to either drain, $V_{CC} - V_D$ . . . . . 33 V
Drain to negative supply voltage, $V_D - V_{EE}$ . . . . . 33 V
Drain to source voltage, $V_D - V_S$ . . . . . ±22 V
Logic supply to negative supply voltage, $V_{LL} - V_{EE}$ . . . . . 36 V
Logic supply to logic input voltage, $V_{LL} - V_I$ . . . . . 33 V
Logic supply to reference voltage, $V_{LL} - V_{ref}$ . . . . . 33 V
Logic input to reference voltage, $V_I - V_{ref}$ . . . . . 33 V
Reference to negative supply voltage, $V_{ref} - V_{EE}$ . . . . . 27 V
Reference to logic input voltage, $V_{ref} - V_I$ . . . . . 2 V
Current (any terminal) . . . . . 30 mA
Operating free-air temperature range: TL182M, TL185M, TL188M, TL191M . . . . −55°C to 125°C
TL182I, TL185I, TL188I, TL191I . . . . . −25°C to 85°C
TL182C, TL185C, TL188C, TL191C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

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electrical characteristics, V_{CC} = 15 V, V_{EE} = −15 V, V_{LL} = 5 V, V_{ref} = 0 V

PARAMETER		TEST CONDITIONS			TL1_M MIN	TL1_M MAX	TL1_I MIN	TL1_I MAX	TL1_C MIN	TL1_C MAX	UNIT
V_{IH}	High-level control input voltage			T_A = MIN TO MAX	V_{ref}+2		V_{ref}+2		V_{ref}+2		V
V_{IL}	Low-level control input voltage			T_A = MIN to MAX		V_{ref}+0.8		V_{ref}+0.8		V_{ref}+0.8	V
I_{IH}	High-level control input current	V_I = 5 V		T_A = 25°C		10		10		20	μA
				T_A = MAX		20		20		20	
I_{IL}	Low-level control input current	V_I = 0		T_A = MIN to MAX		−250		−250		−250	μA
$I_{D(off)}$	Off-state drain current	V_D = 10 V, V_S = −10 V, V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = 25°C				5		5	nA
				T_A = MAX		100		100		100	
$I_{S(off)}$	Off-state source current	V_D = −10 V, V_S = 10 V, V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = 25°C				5		5	nA
				T_A = MAX		100		100		100	
$I_{D(on)}$ + $I_{S(on)}$	On-state channel leakage current	V_D = −10 V, V_S = −10 V, V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = 25°C				−10		−10	nA
				T_A = MAX		−200		−200		−200	
$r_{DS(on)}$	Drain-to-source on-state resistance	V_D = −10 V, I_S = 1 mA, V_{IH} = 2 V, V_{IL} = 0.8 V	TL182, TL188	T_A = MIN to 25°C		75		100		100	Ω
				T_A = MAX		100		150		150	
			TL185, TL191	T_A = MIN to 25°C		125		150		150	
				T_A = MAX		250		300		300	
I_{CC}	Supply current from V_{CC}	Both control inputs at 0 V		T_A = 25°C		1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					−5		−5		−5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					−2		−2		−2	
I_{CC}	Supply current from V_{CC}	Both control inputs at 5 V		T_A = 25°C		1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					−5		−5		−5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					−2		−2		−2	

switching characteristics, V_{CC} = 10 V, V_{EE} = −20 V, V_{LL} = 5 V, V_{ref} = 0 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TL1_M TYP	TL1_I TYP	TL1_C TYP	UNIT
t_{on}	Turn-on time	R_L = 300 Ω, C_L = 30 pF, Figure 1	175	175	175	ns
t_{off}	Turn-off time		350	350	350	

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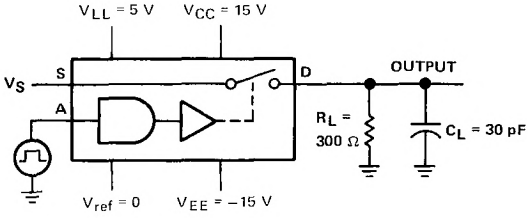
PARAMETER MEASUREMENT INFORMATION

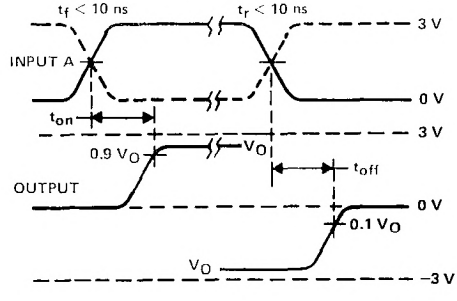


C_L includes probe and jig capacitance

V_S = 3 V for t_{on} and −3 V for t_{off}

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

TEST CIRCUIT



NOTE: A. The solid waveform applies for TL185 and SW1 of TL185 and TL191; the dashed waveform applies for TL182 and SW2 of TL185 and TL191.

B. V_O is the steady-state output with the switch on. Feed through via the gate capacitance may result in spikes (not shown) at the leading and trailing edges of the output waveform.

FIGURE 1. VOLTAGE WAVEFORMS

D2477 DECEMBER 1979—REVISED JANUARY 1989

TL500I, TL500C, TL501I, TL501C ANALOG PROCESSORS

- True Differential Inputs
- Automatic Zero
- Automatic Polarity
- **High Input Impedance . . . 10^9 Ohms** Typically

TL500I, TL500C CAPABILITIES

- Resolution . . .14 Bits (with TL502C)
- Linearity Error . . . 0.001%
- 4 1/2-Digit Readout Accuracy with External Precision Reference

TL501I, TL501C CAPABILITIES

- Resolution . . . 10-13 Bits (with TL502C)
- Linearity Error . . . 0.01%
- 3 1/2-Digit Readout Accuracy

TL502C/TL503C DIGITAL PROCESSORS

- Fast Display Scan Rates
- Internal Oscillator May Be Driven or Free-Running
- Interdigit Blanking
- Over-Range Blanking
- 4 1/2-Digit Display Circuitry
- High-Sink-Current Digit Driver for Large Displays

TL502C CAPABILITIES

- Compatible with Popular Seven-Segment Common-Anode Displays
- High-Sink-Current Segment Driver for Large Displays

TL503C CAPABILITIES

- Multiplexed BCD Outputs
- High-Sink-Current BCD Outputs

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates

description

The TL500I, TL500C, TL501I, and TL501C analog processors and TL502C and TL503C digital processors provide the basic functions for a dual-slope-integrating analog-to-digital converter.

The TL500 and TL501 contain the necessary analog switches and decoding circuits, reference voltage generator, buffer, integrator, and comparator. These devices may be controlled by the TL502C, TL503C, by discrete logic, or by a software routine in a microprocessor.

The TL502C and TL503C each includes oscillator, counter, control logic, and digit enable circuits. The TL502C provides multiplexed outputs for seven-segment displays, while the TL503C has multiplexed BCD outputs.

When used in complementary fashion, these devices form a system that features automatic zero-offset compensation, true differential inputs, high input impedance, and capability for 4 1/2-digit accuracy. Applications include the conversion of analog data from high-impedance sensors of pressure, temperature, light, moisture, and position. Analog-to-digital-logic conversion provides display and control signals for weight scales, industrial controllers, thermometers, light-level indicators, and many other applications.

principles of operation

The basic principle of dual-slope-integrating converters is relatively simple. A capacitor, C_X, is charged through the integrator from V_{CT} for a fixed period of time at a rate determined by the value of the unknown voltage input. Then the capacitor is discharged at a fixed rate (determined by the reference voltage) back to V_{CT} where the discharge time is measured precisely. The relationship of the charge and discharge values are shown below (see Figure 1).

$$V_{CX} = V_{CT} - \frac{V_I t_1}{R_X C_X} \qquad \text{Charge} \qquad (1)$$

$$V_{CT} = V_{CX} - \frac{V_{ref}\, t_2}{R_X C_X} \qquad \text{Discharge} \qquad (2)$$

Combining equations 1 and 2 results in:

$$\frac{V_I}{V_{ref}} = -\frac{t_2}{t_1} \qquad (3)$$

where:

V_{CT} = Comparator (offset) threshold voltage
V_{CX} = Voltage change across C_X during t_1 and during t_2 (equal in magnitude)
V_I = Average value of input voltage during t_1
t_1 = Time period over which unknown voltage is integrated
t_2 = Unknown time period over which a known reference voltage is integrated.

Equation (3) illustrates the major advantages of a dual-slope converter:

a. Accuracy is not dependent on absolute values of t_1 and t_2, but is dependent on their ratios. Long-term clock frequency variations will not affect the accuracy.
b. Offset values, V_{CT}, are not important.

The BCD counter in the digital processor (see Figure 2) and the control logic divide each measurement cycle into three phases. The BCD counter changes at a rate equal to one-half the oscillator frequency.

auto-zero phase

The cycle begins at the end of the integrate-reference phase when the digital processor applies low levels to inputs A and B of the analog processor. If the trigger input is at a high level, a free-running condition exists and continuous conversions are made. However, if the trigger input is low, the digital processor stops the counter at 20,000, entering a hold mode. In this mode, the processor samples the trigger input every 4000 oscillator pulses until a high level is detected. When this occurs, the counter is started again and is carried to completion at 30,000. The reference voltage is stored on reference capacitor C_{ref}, comparator offset voltage is stored on integration capacitor C_X, and the sum of the buffer and integrator offset voltages is stored on zero capacitor C_Z. During the auto-zero phase, the comparator output is characterized by an oscillation (limit cycle) of indeterminate waveform and frequency that is filtered and d-c shifted by the level shifter.

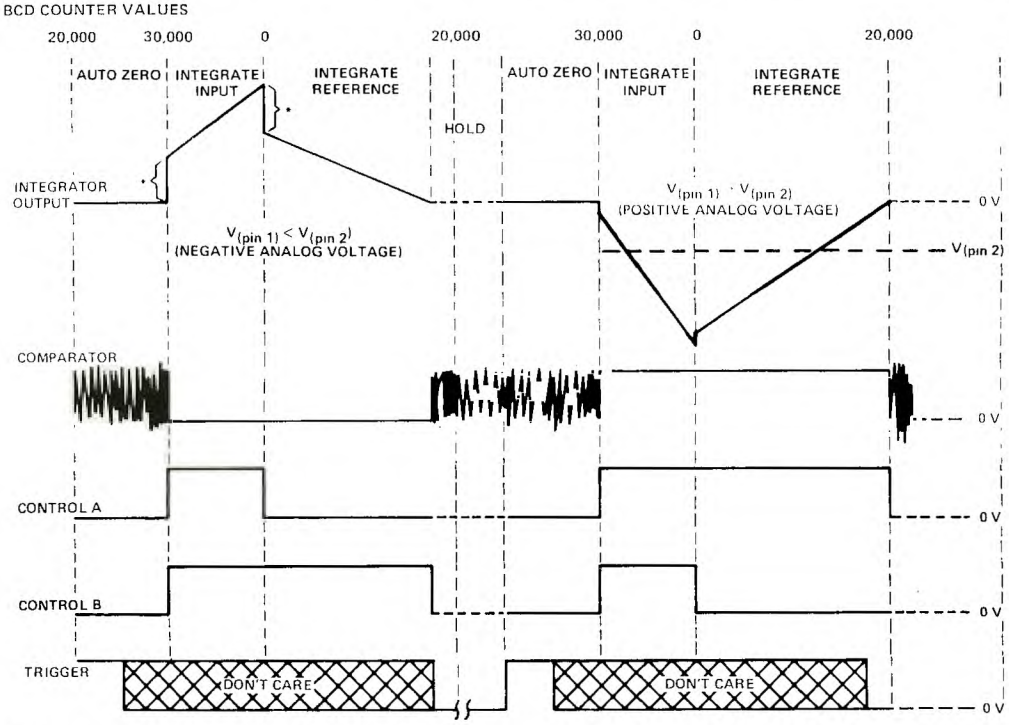
integrate-input phase

The auto-zero phase is completed at a BCD count of 30,000, and high levels are applied to both control inputs to initiate the integrate-input phase. The integrator charges C_X for a fixed time of 10,000 BCD counts at a rate determined by the input voltage. Note that during this phase, the analog inputs see only the high impedance of the noninverting operational amplifier input. Therefore, the integrator responds only to the difference between the analog input terminals, thus providing true differential inputs.

integrate-reference phase

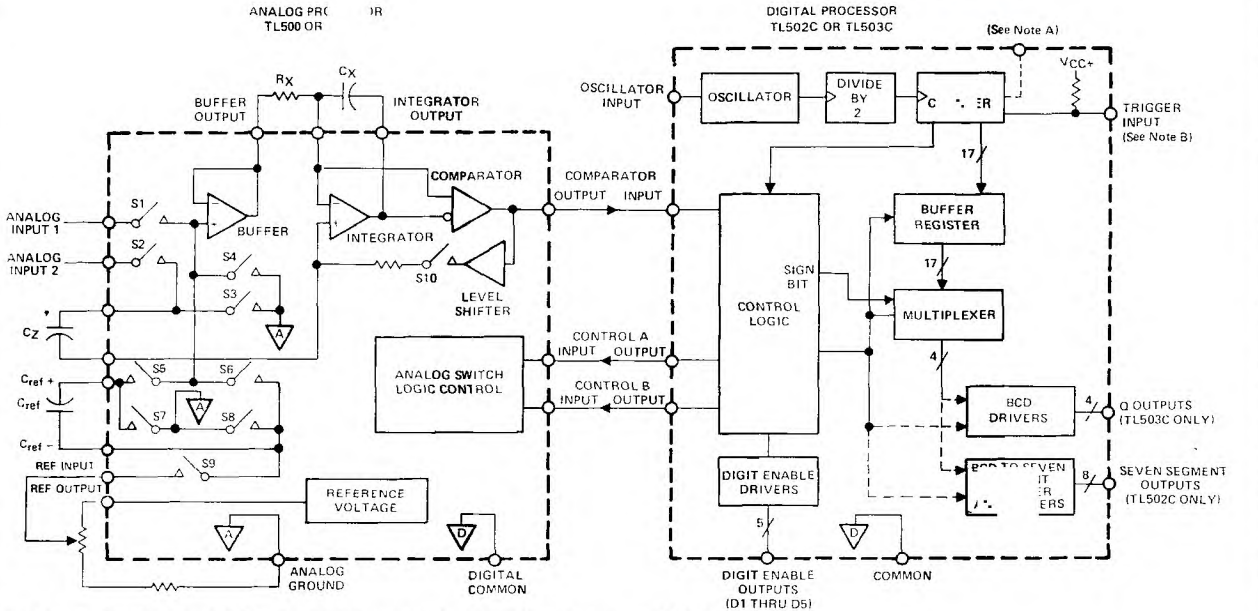
At a BCD count of 39,999 + 1 = 40,000 or 0, the integrate-input phase is terminated and the integrate-reference phase is begun by sampling the comparator output. If the comparator output is low corresponding to a negative average analog input voltage, the digital processor applies a low and a high to inputs A and B, respectively, to apply the reference voltage stored on C_{ref} to the buffer. If the comparator output is high corresponding to a positive input, inputs A and B are made high and low, respectively, and the negative of the stored reference voltage is applied to the buffer. In either case, the processor automatically selects the proper logic state to cause the integrator to ramp back toward zero at a rate proportional to the reference voltage. The time required to return to zero is measured by the counter in the digital processor. The phase is terminated when the integrator output crosses zero and the counter contents are transferred to the register, or when the BCD counter reaches 20,000 and the over-range indication is activated. When activated, the over-range indication blanks all but the most significant digit and sign.

Seventeen parallel bits (4-1/2 digits) of information are strobed into the buffer register at the end of the integration phase. Information for each digit is multiplexed out to the BCD outputs (TL503C) or the seven-segment drivers (TL502C) at a rate equal to the oscillator frequency divided by 200.



*This step is the voltage at pin 2 with respect to analog ground

FIGURE 1. VOLTAGE WAVEFORMS AND TIMING DIAGRAM



NOTES: A. Pin 18 of the TL502C provides an output of f_{osc} (oscillator frequency) – 20,000
B The trigger input assumes a high level if not externally connected

FIGURE 2. BLOCK DIAGRAM OF BASIC ANALOG-TO-DIGITAL CONVERTER USING TL500 OR TL501 AND TL502C OR TL503C

MODE	ANALOG INPUT	COMPARATOR	CONTROLS A AND B	ANALOG SWITCHES CLOSED
Auto Zero	X	Oscillation	L L	S3, S4, S7, S9, S10
Hold†				
Integrate	Positive	H	H H	S1, S2
Input	Negative	L		
Integrate	X	L‡	L H	S3, S6, S7
Reference		H‡	H L	S3, S5, S8

H ≡ High, L ≡ low, X ≡ Irrelevant

† If the trigger input is low at the beginning of the auto-zero cycle, the system will enter the hold mode. A high level (or open circuit) will signal the digital processor to continue or resume normal operation.
‡ This is the state of the comparator output as determined by the polarity of the analog input during the integrate input phase.

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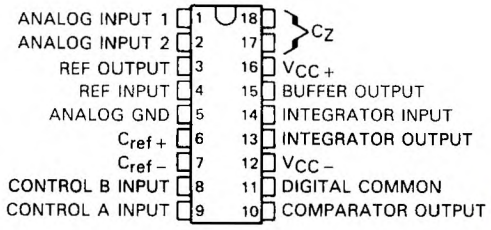
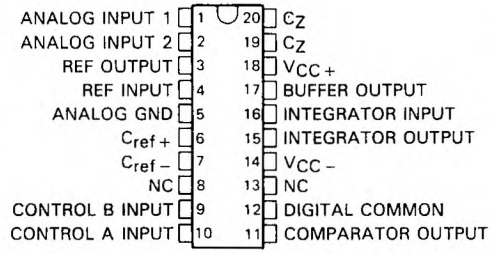
description of analog processors

The TL500 and TL501 analog processors are designed to automatically compensate for internal zero offsets, integrate a differential voltage at the analog inputs, integrate a voltage at the reference input in the opposite direction, and provide an indication of zero-voltage crossing. The external control mechanism may be a microcomputer and software routing, discrete logic, or a TL502C or TL503C controller. The TL500 and TL501 are designed primarily for simple, cost-effective, dual-slope analog-to-digital converters. Both devices feature true differential analog inputs, high input impedance, and an internal reference-voltage source. The TL500 provides 4-1/2-digit readout accuracy when used with a precision external reference voltage. The TL501 provides 100-ppm linearity error and 3-1/2-digit accuracy capability. These devices are manufactured using TI's advanced technology to produce JFET, MOSFET, and bipolar devices on the same chip. The TL500C and TL501C are characterized for operation over the temperature range of 0°C to 70°C. The TL500I and TL501I are characterized for operation from −40°C to 85°C.

J PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)

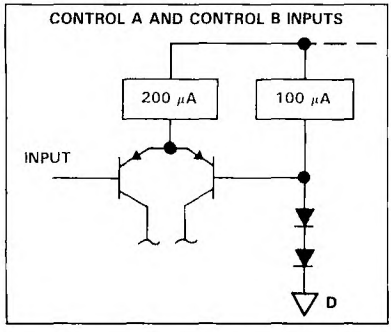


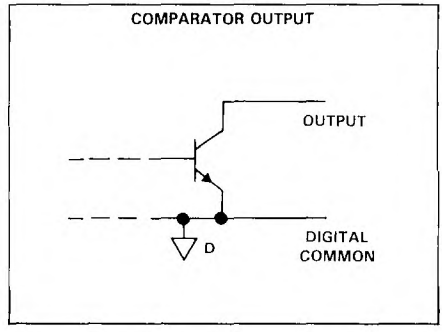
NC – No internal connection

AVAILABLE OPTIONS

T_A	LINEARITY ERROR	PACKAGE	
		CERAMIC DIP (J)	WIDE-BODY SO (DW)
0°C to 70°C	0.005% FS	TL500CJ	TL500CDW
	0.05% FS	TL501CJ	TL501CDW
−40°C to 85°C	0.005% FS	TL500IJ	TL500IDW
	0.05% FS	TL501IJ	TL501IDW

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply voltage, V_{CC+} (see Note 1) . . . . . +18 V
Negative supply voltage, V_{CC-} . . . . . −18 V
Input voltage, V_I . . . . . $\pm V_{CC}$
Comparator output voltage range (see Note 2) . . . . . 0 V to V_{CC+}
Comparator output sink current (see Note 2) . . . . . 20 mA
Buffer, reference, or integrator output source current (see Note 2) . . . . . 10 mA
Total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TL500I, TL501I . . . . . −40 to 85°C
TL500C, TL501C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES. 1. Voltage values, except differential voltages, are with respect to the analog ground common pin tied together.
2. Buffer, integrator, and comparator outputs are not short-circuit protected.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9 mW/°C	720 mW	585 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW

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recommended operating conditions

		MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC+}		7	12	15	V
Negative supply voltage, V_{CC-}		−9	−12	−15	V
Reference input voltage, $V_{ref(I)}$		0.1		5	V
Analog input voltage, V_I				±5	V
Differential analog input voltage, V_{ID}				10	V
High-level input voltage, V_{IH}	Control inputs	2			V
Low-level input voltage, V_{IL}	Control inputs			0.8	V
Peak positive integrator output voltage, V_{OM+}		+9			V
Peak negative integrator output voltage, V_{OM-}		−5			V
Full scale input voltage				2 V_{ref}	
Autozero and reference capacitors, C_Z and C_{ref}		0.2			μF
Integrator capacitor, C_X		0.2			μF
Integrator resistor, R_X		15		100	kΩ
Integrator time constant, R_XC_X		See Note 3			
Free-air operating temperature, T_A	TL500I, TL501I	−40		85	°C
	TL500C, TL501C	0		70	
Maximum conversion rate with TL502C or TL503C			3	12.5	conv/sec

system electrical characteristics at $V_{CC\pm}$ = ±12 V, V_{ref} = 1,000 ± 0.03 mV, T_A = 25°C (unless otherwise noted) (see Figure 3)

PARAMETER	TEST CONDITIONS	TL501			TL500			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero error			50	300		10	30	μV
Linearity error relative to full scale	V_I = 2 V to 2 V		0.005	0.05		0.001	0.005	%FS
Full scale temperature coefficient	T_A = full range		6			6		ppm/°C
Temperature coefficient of zero error			4			1		μV/°C
Rollover error†				500		30	100	μV
Equivalent peak-to-peak input noise voltage			20			20		μV
Analog input resistance	Pin 1 or 2		10^9			10^9		Ω
Common-mode rejection ratio	V_{IC} = −1 V to +1 V		86			90		dB
Current into analog input	V_I = ±5 V		50			50		pA
Supply voltage rejection ratio			90			90		dB

†Rollover error is the voltage difference between the conversion results of the full-scale positive 2 V and the full-scale negative 2 V.

NOTE 3. The minimum integrator time constant may be found by use of the following formula:

$$\text{Minimum } R_XC_X = \frac{V_{ID}\ (\text{full scale})\ t_1}{V_{OM-} - V_I(\text{pin 2})}$$

where

V_{ID} = voltage at pin with respect to pin 2
V_I(pin 2) = voltage at pin 2 with respect to analog ground
t_1 = input integration time seconds

electrical characteristics at $V_{CC\pm}$ = ±12 V, V_{ref} = 1 V, T_A = 25°C (see Figure 3)

integrator and buffer operational amplifiers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage			15		mV
I_{IB}	Input bias current			50		pA
V_{OM+}	Positive output voltage swing		9	11		V
V_{OM-}	Negative output voltage swing		−5	−7		V
A_{VD}	Voltage amplification			110		dB
B_1	Unity-gain bandwidth			3		MHz
CMRR	Common mode rejection	V_{IC} = −1 V to +1 V		100		dB
SR	Output slew rate			5		V/μs

comparator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage			15		mV
I_{IB}	Input bias current			50		pA
A_{VD}	Voltage amplification			100		dB
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		200	400	mV
I_{OH}	High-level output current	V_{OH} = 3 V		5	20	nA

voltage reference output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ref(0)}$	Reference voltage		1.12	1.22	1.32	V
αV_{ref}	Reference-voltage temperature coefficient	T_A = full range		80		ppm/°C
r_o	Reference output resistance			3		Ω

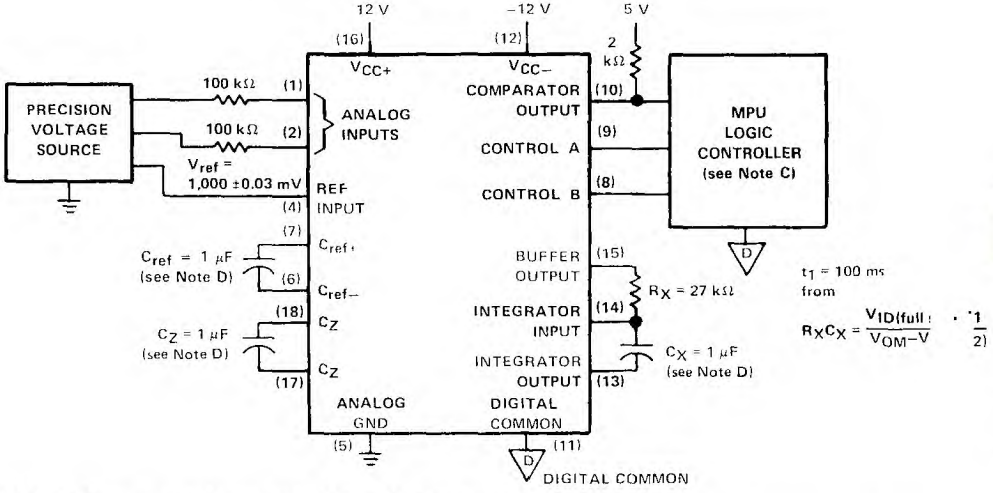
logic control section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	V_{IH} = 2 V		1	10	μA
I_{IL}	Low-level input current	V_{IL} = 0.8 V		−40	−300	μA

total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC+}	Positive supply current			15	20	mA
I_{CC-}	Negative supply current			12	18	mA

PARAMETER MEASUREMENT INFORMATION



NOTES: C. Tests are started approximately 5 seconds after power-on.

D. Capacitors used are TRW's X363UW polypropylene or equivalent for C_X, C_{ref}, and C_Z; however for C_{ref} and C_Z film-dielectric capacitors may be substituted

FIGURE 3. TEST CIRCUIT CONFIGURATION

external-component selection guide

The autozero capacitor C_Z and reference capacitor C_{ref} should be within the recommended range of operating conditions and should have low-leakage characteristics. Most film-dielectric capacitors and some tantalum capacitors provide acceptable results. Ceramic and aluminum capacitors are not recommended because of their relatively high-leakage characteristics.

The integrator capacitor C_X should also be within the recommended range and must have good voltage linearity and low dielectric absorption. A polypropylene-dielectric capacitor similar to TRW's X363UW is recommended for 4-1/2-digit accuracy. For 3-1/2-digit applications, polyester, polycarbonate, and other film dielectrics are usually suitable. Ceramic and electrolytic capacitors are not recommended.

Stray coupling from the comparator output to any analog pin (in order of importance 17, 18, 14, 7, 6, 13, 1, 2, 15) must be minimized to avoid oscillations. In addition, all power supply pins should be bypassed at the package, for example, by a 0.01-μF ceramic capacitor.

Analog and digital common are internally isolated and may be at different potentials. Digital common can be within 4 V of positive or negative supply with the logic decode still functioning properly.

The time constant R_XC_X should be kept as near the minimum value as possible and is given by the formula:

$$\text{Minimum } R_XC_X = \frac{V_{ID}\ (\text{full scale})\ t_1}{V_{OM-} - V_{I(pin2)}}$$

where:

$V_{ID(full\ scale)}$ = Voltage on pin 1 with respect to pin 2
t_1 = Input integration time in seconds
$V_{I(pin2)}$ = Voltage on pin 2 with respect to analog ground.

description of digital processors

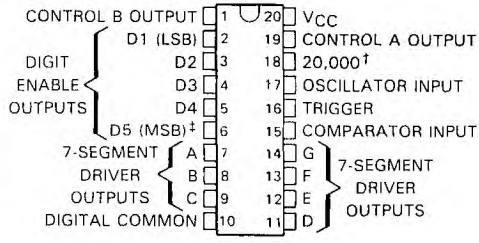
The TL502C and TL503C are control logic devices designed to complement the TL500 and TL501 analog processors. They feature interdigit blanking, over-range blanking, an internal oscillator, and a fast display scan rate. The internal-oscillator input is a Schmitt trigger circuit that can be driven by an external clock pulse or provide its own time base with the addition of a capacitor. The typical oscillator frequency is 120 kHz with a 470-pF capacitor connected between the oscillator input and ground.

The TL502C provides seven-segment-display output drivers capable of sinking 100 mA and compatible with popular common-anode displays. The TL503C has four BCD output drivers capable of 100-mA sink currents. The code (see next page and Figure 4) for each digit is multiplexed to the output drivers in phase with a pulse on the appropriate digit-enable line at a digit rate equal to f_{osc}, divided by 200. Each digit-enable output is capable of sinking 20-mA.

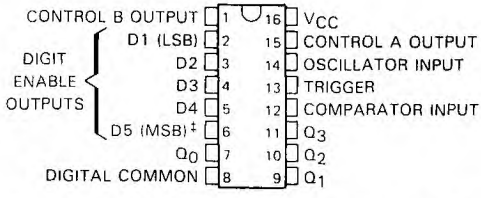
The comparator input of each device, in addition to monitoring the output of the zero-crossing detector in the analog processor, may be used in the display test mode to check for wiring and display faults. A high logic level (2 to 6.5 V) at the trigger input with the comparator input at or below 6.5 V starts the integrate-input phase. Voltage levels equal to or greater than 7.9 V on both the trigger and comparator inputs clear the system and set the BCD counter to 20,000. When normal operation resumes, the conversion cycle is restarted at the auto zero phase.

These devices are manufactured using I^2L and bipolar techniques. The TL502C and TL503C are characterized for operation from 0°C to 70°C.

TL502C . . . N PACKAGE
(TOP VIEW)



TL503C . . . N PACKAGE
(TOP VIEW)



†Pin 18 of TL502C provides an output of f_{osc} (oscillator frequency) – 20,000.
‡D5, the most significant bit, is also the sign bit

TABLE OF SPECIAL FUNCTIONS
V_{CC} = 5 V ±10%

TRIGGER INPUT	COMPARATOR INPUT	FUNCTION
$V_I \leq 0.8$ V	$V_I \leq 6.5$ V	Hold at auto-zero cycle after completion of conversion
2 V $\leq V_I \leq$ 6.5 V	$V_I \leq 6.5$ V	Normal operation (continuous conversion)
$V_I \leq 6.5$ V	$V_I \geq 7.9$ V	Display Test: All BCD outputs high
$V_I \geq 7.9$ V	$V_I \leq 6.5$ V	Internal Test
Both inputs to go $V_I \geq 7.9$ V simultaneously		System clear: Sets BCD counter to 20,000. When normal operation is resumed, cycle begins with Auto Zero.

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DIGIT 5 (MOST SIGNIFICANT DIGIT) CHARACTER CODES

CHARACTER	TL502C SEVEN-SEGMENT LINES							TL503C BCD OUTPUT LINES			
	A	B	C	D	E	F	G	Q3	Q2	Q1	Q0
								8	4	2	1
+	H	H	H	H	L	L	L	H	L	H	L
+1	H	L	L	H	L	L	L	H	H	H	L
−	L	H	H	L	H	H	L	H	L	H	H
−1	L	L	L	L	H	H	L	H	H	H	H

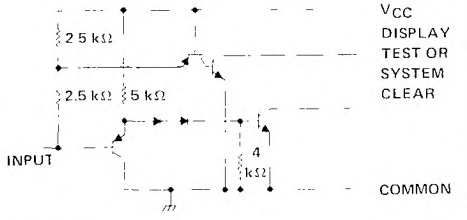
DIGITS 1 THRU 4 NUMERIC CODE (See Figure 4)

NUMBER	TL502C SEVEN-SEGMENT LINES							TL503C BCD OUTPUT LINES			
	A	B	C	D	E	F	G	Q3	Q2	Q1	Q0
								8	4	2	1
0	L	L	L	L	L	L	H	L	L	L	L
1	H	L	L	H	H	H	H	L	L	L	H
2	L	L	H	L	L	H	L	L	L	H	L
3	L	L	L	L	H	H	L	L	L	H	H
4	H	L	L	H	H	L	L	L	H	L	L
5	L	H	L	L	H	L	L	L	H	L	H
6	L	H	L	L	L	L	L	L	H	H	L
7	L	L	L	H	H	H	H	L	H	H	H
8	L	L	L	L	L	L	L	H	L	L	L
9	L	L	L	L	H	L	L	H	L	L	H

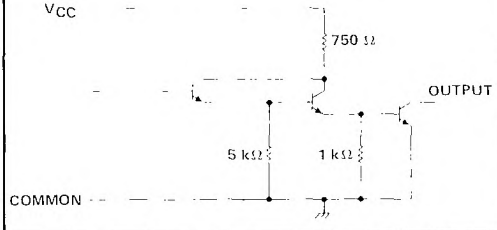
H = high level, L = low level

schematics of inputs and outputs

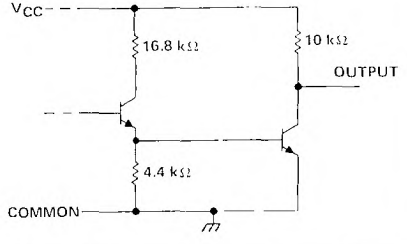
COMPARATOR AND TRIGGER INPUT



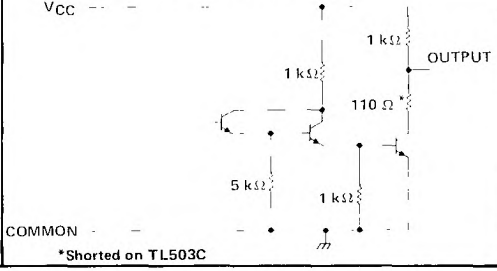
SEGMENT DRIVERS—TL502C
BCD DRIVERS—TL503C



CONTROL A AND B OUTPUTS



DIGIT-ENABLE OUTPUTS



*Shorted on TL503C

absolute maximum ratings

Supply voltage, V_{CC} (see Note 4)		7	V
Input voltage, V_I	Oscillator	5.5	V
	Comparator or Trigger	.9	
Output current	BCD or Segment drivers	120	mA
	Digit-enable · uts	40	
	Pin 18 (TLE . only)	20	
Total power dissipation at (or below) 30°C free-air temperature (see Note 5)		1100	mW
Operating free-air temperature range		0 to 70	°C
Storage temperature range		−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

NOTES: 4. Voltage values are with respect to the network ground terminal.
5. For operation above 30°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	Comparator and trigger inputs	2			V
Low-level input voltage, V_{IL}	Comparator and trigger inputs			0.8	V
Operating free-air temperature		0		70	°C

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electrical characteristics at 25°C free-air temperature

PARAMETER		TERMINAL	TEST CONDITIONS		TL502C			TL503C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IK}	Input clamp voltage	All inputs	V_{CC} = 4.5 V,	I_I = −12 mA		−0.8	−1.5		−0.8	−1.5	V
V_{T+}	Positive-going input threshold voltage	Oscillator	V_{CC} = 5 V			1.5			1.5		V
V_{T-}	Negative-going input threshold voltage	Oscillator	V_{CC} = 5 V			0.9			0.9		V
$V_{T+} - V_{T-}$	Hysteresis	Oscillator	V_{CC} = 5 V		0.4	0.6	0.8	0.4	0.6	0.8	
I_{T-}	Input current at positive-going input threshold voltage	Oscillator	V_{CC} = 5 V		−40	−94	−170	−40	−94	−170	μA
I_{T-}	Input current at negative-going input threshold voltage	Oscillator	V_{CC} = 5 V		40	117	170	40	117	170	μA
V_{OH}	High-level output voltage	Digit enable	V_{CC} = 4.5 V,	I_{OH} = 0	4.15	4.4		4.15	4.4		V
		Pin 18 (TL502C only)			4.25	4.4					
		Control A and B			4.25	4.4		4.25	4.4		
V_{OL}	Low-level output voltage	Digit enable	V_{CC} = 4.5 V	I_{OL} = 20 mA					0.2	0.5	V
		Pin 18 (TL502C only)		I_{OL} = 10 mA		0.15	0.4				
		Control A and B		I_{OL} = 2 mA		0.088	0.4		0.088	0.4	
		Segment drivers		I_{OL} = 100 mA		0.17	0.3				
		BCD drivers		I_{OL} = 100 mA					0.17	0.3	
I_I	Input current	Comparator, Trigger	V_{CC} = 5.5 V,	V_I = 5.5 V		65	100		65	100	μA
		Oscillator					1			1	mA
I_{IH}	High-level input current	Comparator, Trigger	V_{CC} = 5.5 V,	V_I = 2.4 V		0.6	1		0.6	1	mA
		Oscillator					0.5			0.5	
I_{IL}	Low-level input voltage	Oscillator	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.1	−0.17		−0.1	−0.17	mA
		Comparator, Trigger				−1	−1.6		−1	−1.6	
I_{OH}	High-level output current (Output transistor off)	Digit enable	V_{CC} = 4.5 V	V_O = 0.5 V,	−2.5	−4		−2.5	−4		mA
		Pin 18 (TL502C only)		V_O = 0.5 V	−0.5	−0.9					
		Control A and B		V_O = 0.5 V	−0.25	−0.4		−0.25	−0.4		
		Segment drivers		V_O = 5.5 V			0.25				
		BCD drivers		V_O = 5.5 V						0.25	
I_{OL}	Low-level output current (Output transistor on)	Digit enable	V_{CC} = 4.5 V,	V_O = 3.55 V	18	23					mA
I_{CC}	Supply current	V_{CC}	V_{CC} = 5.5 V			73	110		73	110	mA

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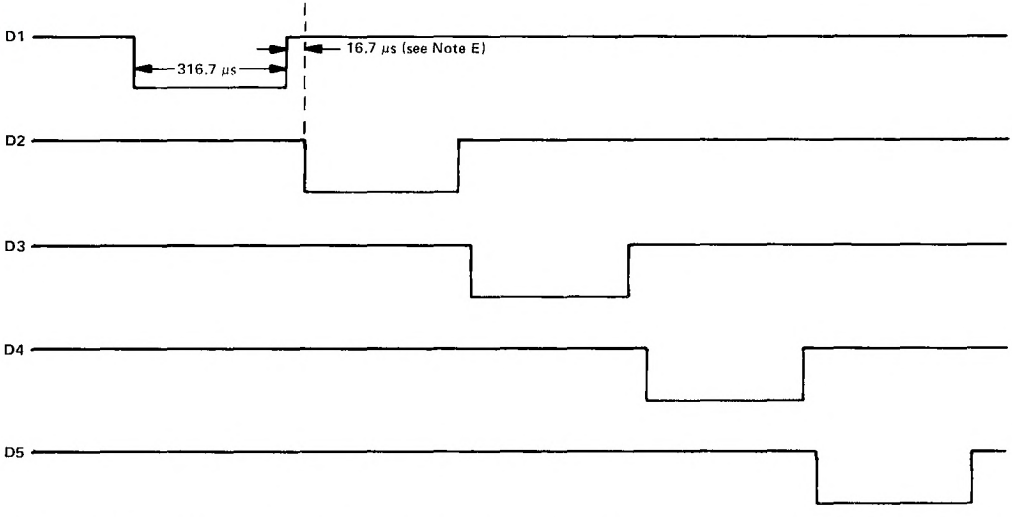
special functions† operating characteristics at 25 °C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current into comparator or trigger inputs	V_{CC} = 5.5 V, V_I = 8.55 V		1.2	1.8	mA
		V_{CC} = 5.5 V, V_I = 6.25 V			0.5	mA

†The comparator and trigger inputs may be used in the normal mode or to perform special functions. See the Table of Special Functions.

TYPICAL APPLICATION DATA



NOTE E: The BCD or seven-segment driver outputs are present for a particular digit slightly before the falling edge of that digit enable.

FIGURE 4. TL502C, TL503C DIGIT TIMING WITH 120-kHz CLOCK SIGNAL AT OSCILLATOR INPUT

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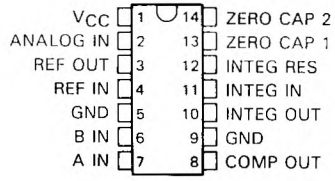
D2366, OCTOBER 1977 – REVISED FEBRUARY 1989

- 3-Digit Accuracy (0.1%)
- 10-Bit Resolution
- Automatic Zero
- Internal Reference Voltage
- Single-Supply Operation
- High-Impedance MOS Input
- **Designed for Use with TMS1000 Type Microprocessors for Cost-Effective High-Volume Applications**
- BI-MOS Technology
- Only 40 mW Typical Power Consumption

N PACKAGE
(TOP VIEW)



Caution. This device has limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

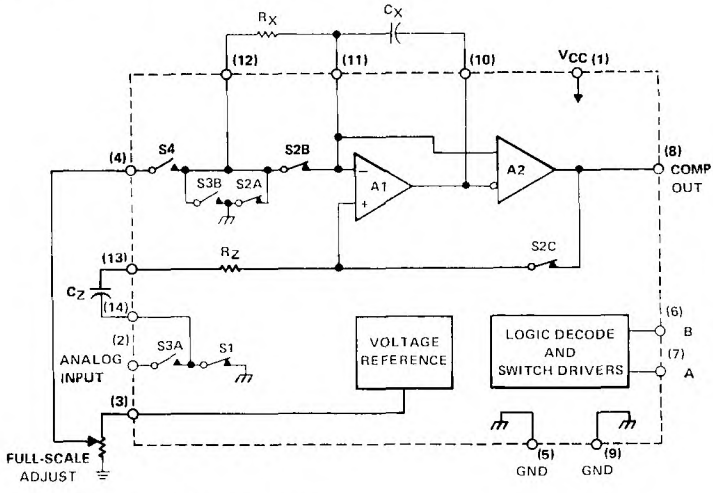
description

The TL505C is an analog-to-digital converter building block designed for use with TMS1000 type microprocessors. It contains the analog elements (operational amplifier, comparator, voltage reference, analog switches, and switch drivers) necessary for a unipolar automatic-zeroing dual-slope converter. The logic for the dual-slope conversion can be performed by the associated MPU as a software routine or can be implemented with other components, such as the TL502 logic-control device.

The high-impedance MOS inputs permit the use of less expensive, lower value capacitors for the integration and offset capacitors and permit conversion speeds from 20 per second to 0.05 per second.

The TL505C is a product of TI's BI-MOS process, which incorporates bipolar and MOSFET transistors on the same monolithic circuit. The TL505C is characterized for operation from 0°C to 70°C.

functional block diagram



NOTE: Analog and digital GND are internally connected together.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Input voltage, pins 2, 4, 6, and 7 . . . . . V_{CC}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to the two ground terminals connected together.
2. For operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	7	9	15	V
Analog input voltage, V_I	0		4	V
Reference input voltage, $V_{ref(I)}$	0.5		3	V
High-level input voltage at A or B, V_{IH}	3.6		$V_{CC}+1$	V
Low-level input voltage at A or B, V_{IL}	0.2		1.8	V
Integrator capacitor, C_X	See "component selection"			
Integrator resistor, R_X	0.5		2	MΩ
Integration time, t_1	16.6		500	ms
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, V_{CC} = 9 V, $V_{ref(I)}$ = 1 V, T_A = 25°C, connected as shown in Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage at pin 8	I_{OH} = 0	7.5	8.5		V
I_{OH}	High-level output current at pin 8	V_{OH} = 7.5 V		−100		μA
V_{OL}	Low-level output voltage at pin 8	I_{OL} = 1.6 mA		200	400	mV
V_{OM}	Maximum peak output voltage swing at integrator output	$R_X \geq 500$ kΩ	$V_{CC}-2$	$V_{CC}-1$		V
$V_{ref(0)}$	Reference output voltage	I_{ref} = −100 μA	1.15	1.22	1.35	V
αV_{ref}	Temperature coefficient of reference output voltage	T_A = 0°C to 70°C		±100		ppm/°C
I_{IH}	High-level input current into A or B	V_I = 9 V		1	10	μA
I_{IL}	Low-level input current into A or B	V_I = 1 V		10	200	μA
I_I	Current into analog input	V_I = 0 to 4 V, A input at 0 V		±10	±200	pA
I_{IB}	Total integrator input bias current			±10		pA
I_{CC}	Supply current	No load		4.5	8	mA

system electrical characteristics, V_{CC} = 9 V, $V_{ref(I)}$ = 1 V, T_A = 25°C, connected as shown in Figure 1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero error	V_I = 0		0.1	0.4	mV
Linearity error	V_I = 0 to 4 V		0.02	0.1	%FS
Ratiometric reading	$V_I = V_{ref(I)} \approx 1$ V	0.998	1.000	1.002	
Temperature coefficient of ratiometric reading	$V_{ref(I)}$ constant and ≈ 1 V, T_A = 0°C to 70°C		±10		ppm/°C

DEFINITION OF TERMS

Zero Error

The intercept (b) of the anolog-to-digital converter system transfer function y = mx + b, where y is the digital output, x is the analog input, and m is the slope of the transfer function, which is approximated by the ratiometric reading.

Linearity Error

The maximum magnitude of the deviation from a straight line between the end points of the transfer function.

Ratiometric Reading

The ratio of negative integration time (t_2) to positive time (t_1).

PRINCIPLES OF OPERATION

A block diagram of an MPU system using the TL505C is shown in Figure 1. The TL505C operates in a modified positive-integration, three-step, dual-slope conversion mode. The A/D converter waveforms during the conversion process are illustrated in Figure 2.

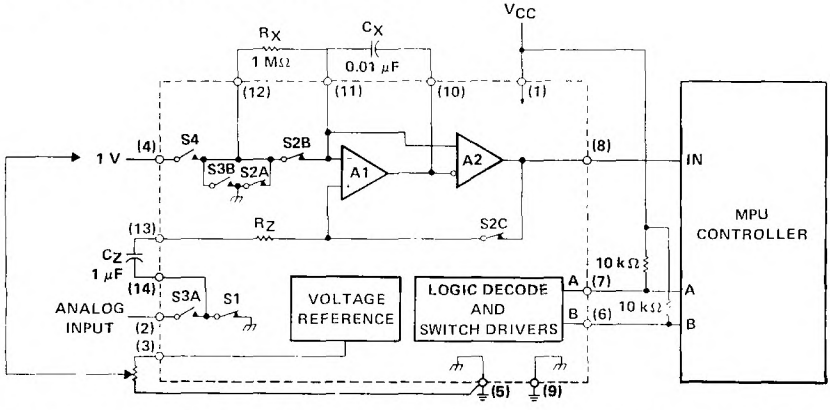
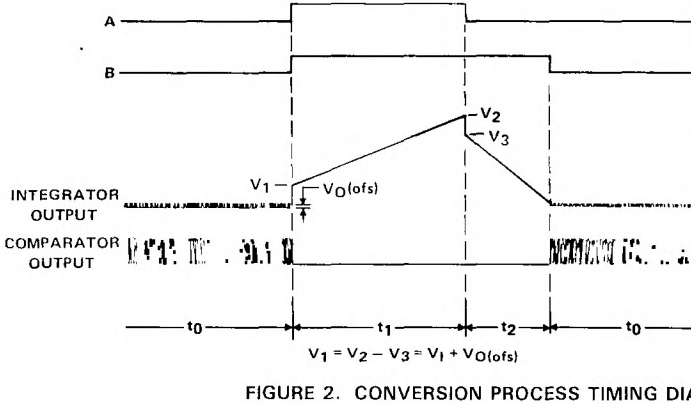


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF TL505C INTERFACE WITH A MICROPROCESSOR SYSTEM



FUNCTION TABLE

CONTROLS A	CONTROLS B	ANALOG SWITCHES CLOSED
L	L	S1, S2
H	H	S3
L	H	S1, S4

H = V_{IH}, L = V_{IL}

FIGURE 2. CONVERSION PROCESS TIMING DIAGRAMS

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PRINCIPLES OF OPERATION (Continued)

The first step of the conversion process is the auto-zero period t_0. By the end of this period, the integrator offset is stored in the autozero capacitor, and the offset of the comparator is stored in the integrator capacitor. To achieve this end, the MPU takes the A and B inputs low, which closes S1 and S2. The output of the comparator is connected to the input of the integrator through the low-pass filter consisting of R_Z and C_Z. The closed loop of A1 and A2 seeks a null condition in which the offsets of the integrator and comparator are stored in C_Z and C_X, respectively. This null condition is characterized by a high-frequency oscillation at the output of the comparator. The purpose of S2B is to shorten the amount of time required to reach the null condition.

At the conclusion of t_0, the MPU takes the A and B inputs both high, which closes S3 and opens all other switches. The input signal V_I is applied to the noninverting input of A1 through C_Z. V_I is then positively integrated by A1. Since the offset of A1 is stored in C_Z, the change in voltage across C_X is due to only the input voltage. Since the input is integrated in a positive integration during t_1, the output of A1 will be the sum of the input voltage, the integral of the input voltage, and the comparator offset, as shown in Figure 2. The change in voltage across capacitor C_X (V_{CX}) during t_1 is given by

$$\Delta V_{CX(1)} = \frac{V_I t_1}{R_1 C_X} \tag{1}$$

where $R_1 = R_X + R_{S3B}$ and R_{S3B} is the resistance of switch S3B.

At the end of t_1, the MPU takes the A input low and the B input high, which closes S1 and S4 and opens all other switches. In this state, the reference is integrated by A1 in a negative sense until the integrator output reaches the comparator threshold. At this point, the comparator output goes high. This change in state is sensed by the MPU, which terminates t_2 by again taking the A and B inputs both low. During t_2, the change in voltage across C_X is given by

$$\Delta V_{CX(2)} = \frac{V_{ref} t_2}{R_2 C_X} \tag{2}$$

where $R_2 = R_X + R_{S4} + R_{ref}$ and R_{ref} is the equivalent resistance of the reference divider.

Since $\Delta V_{CX1} = -\Delta V_{CX2}$, equations (1) and (2) can be combined to give

$$V_I = V_{ref} \frac{R_1 \cdot t_2}{R_2 \cdot t_1} \tag{3}$$

This equation is a variation on the ideal dual-slope equation, which is

$$V_I = V_{ref} \frac{t_2}{t_1} \tag{4}$$

Ideally then, the ratio of R_1/R_2 would be exactly equal to one. In a typical TL505C system where $R_X = 1\ M\Omega$, the scaling error introduced by the difference in R_1 and R_2 is so small that it can be neglected, and equation (3) reduces to (4).

PRINCIPLES OF OPERATION (Continued)

component selection

The autozero capacitor C_Z should be within the recommended range of operating conditions and should have low leakage characteristics. Most film-dielectric capacitors and some tantalum capacitors provide acceptable results. Ceramic and aluminum capacitors are not recommended because of their relatively high leakage characteristics.

The integrator capacitor C_X should also be within the recommended range and must have good voltage linearity and low dielectric absorption. For 10-bit applications, polyster, polycarbonate, and other film dielectrics are usually suitable. If greater precision or stability is required, a polypropylene-dielectric capacitor similar to TRW's X363UW might be appropriate.

Stray coupling from the comparator output to any analog pin (in order of importance, 13, 11, 10, 2, 4) must be minimized to avoid oscillations. In addition, all power supply pins should be bypassed at the package, for example, by a 0.01-μF ceramic capacitor.

The time constant R_XC_X should be kept as near the minimum value as possible and is given by the formula:

$$\text{Minimum } R_XC_X = \frac{V_{I(max)}\, t_1}{(V_{CC} - 2\text{ V} - V_{I(max)})}$$

where:

t_1 = Input integration time in seconds,

$V_{I(max)}$ = the maximum value of the analog input voltage,

$V_{CC} - 2$ V = the maximum voltage swing of the integrator input.

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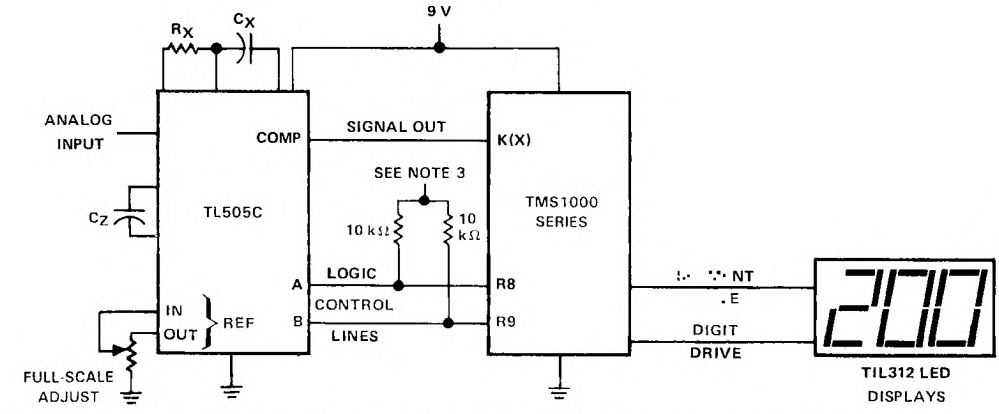
TYPICAL APPLICATION DATA



NOTE 3: Connect to either 9 V or 0 V depending on which device in the TMS1000 series is used and how it is programmed.

FIGURE 3. TL505C IN CONJUNCTION WITH A TMS1000 SERIES MICROPROCESSOR FOR A 3-DIGITAL PANEL METER APPLICATION

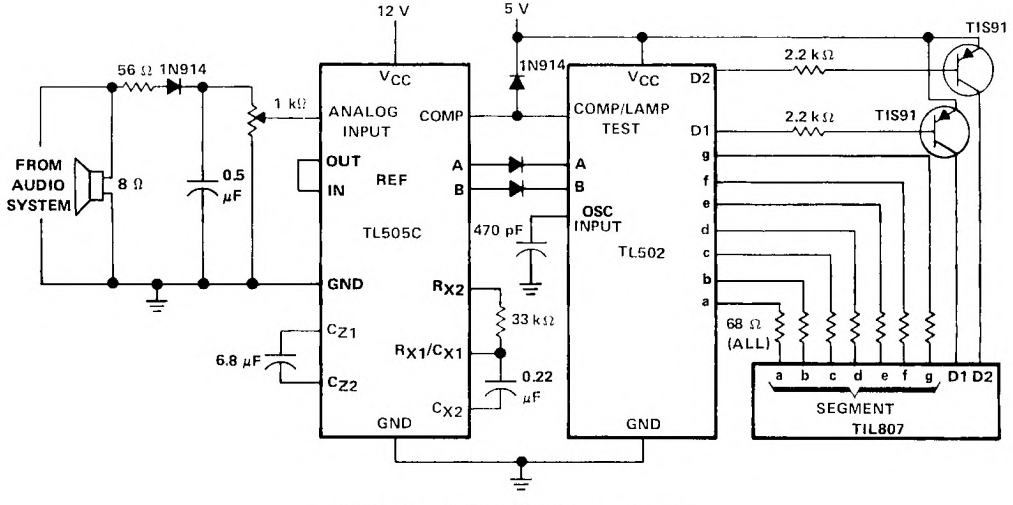
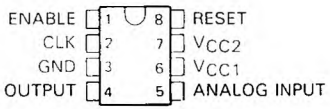


FIGURE 4. AUDIO PEAK POWER METER

D2503, OCTOBER 1979 – REVISED OCTOBER 1988

- Low Cost
- 7-Bit Resolution
- Monotonicity Over Entire A/D Conversion Range
- Ratiometric Conversion
- Conversion Speed . . . Approximately 1 ms
- Single-Supply Operation . . . Either Unregulated 8-V to 18-V (V_{CC2} Input), or Regulated 3.5-V to 6-V (V_{CC1} Input)
- I^2L Technology
- Power Consumption at 5 V . . . 25 mW Typ
- Regulated 5.5 V Output (≤ 1 mA)

P PACKAGE
(TOP VIEW)



FUNCTION TABLE

ANALOG INPUT CONDITION	ENABLE	OUTPUT
X	L†	H
$V_I < 200$ mV	H	L
$V_{ramp} > V_I > 200$ mV	H	H
$V_I > V_{ramp}$	H	L

†Low level on enable also inhibits the reset function.
H = high level, L = low level, X = irrelevant

A high level on the reset pin clears the counter to zero, which sets the internal ramp to 0.75 V_{CC}. Internal pull-down resistors keep the reset and enable pins low when not connected.

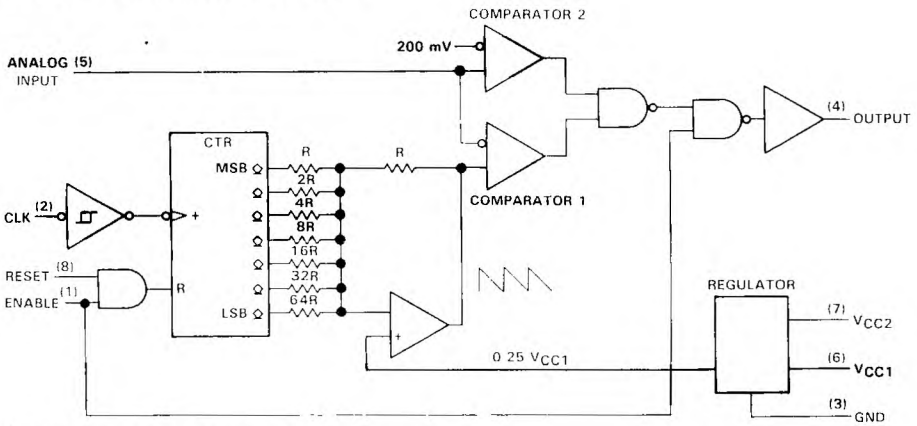
description

The TL507 is a low-cost single-slope analog-to-digital converter designed to convert analog input voltages between 0.25 V_{CC1} and 0.75 V_{CC1} into a pulse-width-modulated output code. The device contains a 7-bit synchronous counter, a binary weighted resistor ladder network, an operational amplifier, two comparators, a buffer amplifier, an internal regulator, and necessary logic circuitry. Integrated-injection logic (I^2L) technology makes it possible to offer this complex circuit at low cost in a small dual-in-line 8-pin package.

In continuous operation, conversion speeds of up to 1000 conversions per second are possible. The TL507 requires external signals for clock, reset, and enable. Versatility and simplicity of operation, coupled with low cost, makes this converter especially useful for a wide variety of applications.

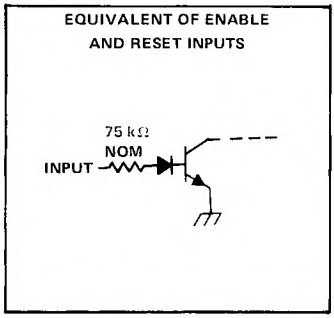
The TL507I is characterized for operation from −40°C to 85°C, and the TL507C is characterized for operation from 0°C to 70°C.

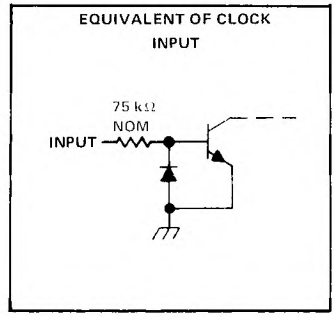
functional block diagram (positive logic)

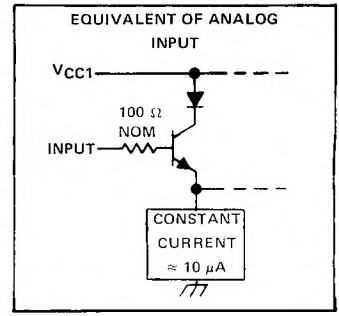


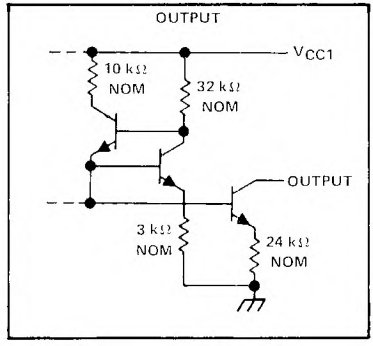
◇indicates an n-p-n open collector output

schematics of inputs and outputs









absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 6.5 V
Supply voltage, V_{CC2} . . . . . 20 V
Input voltage at analog input . . . . . 6.5 V
Input voltage at enable, clock, and reset inputs . . . . . ±20 V
On-state output voltage . . . . . 6 V
Off-state output voltage . . . . . 20 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1000 mW
Operating free-air temperature range: TL507I . . . . . −40°C to 85°C
TL507C . . . . . 0 to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, derate linearly to 520 mW at 85°C at the rate of 8.0 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	3.5	5	6	V
Supply voltage, V_{CC2}	8	15	18	V
Input voltage at analog input	0		5.5	V
Input voltage at chip enable, clock, and reset inputs			±18	V
High-level input voltage, V_{IH}, reset and enable	2			V
Low-level input voltage, V_{IL}, reset and enable			0.8	V
On-state output voltage			5.5	V
Off-state output voltage			18	V
Clock frequency, f_{clock}	0	125	150	kHz

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = V_{CC2} = 5 V (unless otherwise noted)

regulator section

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{CC1}	Supply voltage (output)	V_{CC2} = 10 to 18 V,	I_{CC1} = 0 to −1mA	5	5.5	6	V
I_{CC1}	Supply current	V_{CC1} = 5 V,	V_{CC2} open		5	8	mA
I_{CC2}	Supply current	V_{CC2} = 15 V,	V_{CC1} open		7	10	mA

inputs

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage‡	Clock Input				4.5	V
V_{T-}	Negative-going threshold voltage‡			0.4			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			2	2.6	4	V
I_{IH}	High-level input current	Reset, Enable, and Clock	V_I = 2.4 V		17	35	μA
			V_I = 18 V	130	220	320	
I_{IL}	Low-level input current		V_I = 0			±10	μA
I_I	Analog input current		V_I = 4 V		10	300	nA

output section

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{OH}	High-level output current	V_{OH} = 18 V		0.1	100	μA
I_{OL}	Low-level output current	V_{OL} = 5.5 V	5	10	15	mA
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		80	400	mV

operating characteristics over recommended operating free-air temperature range, V_{CC1} = V_{CC2} = 5.12 V

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Overall error				±80	mV
Differential nonlinearity	See Figure 1			±20	mV
Zero error‡	Binary count = 0			±80	mV
Scale error	Binary count = 127			±80	mV
Full scale input voltage‡	Binary count = 127	3.74	3.82	3.9	V
Propagation delay time from reset or enable			2		μs

†All typical values are at T_A = 25°C.
‡These parameters are linear functions of V_{CC1}.

definitions

zero error

The absolute value of the difference between the actual analog voltage at the 01H-to-00H transition and the ideal analog voltage at that transition.

overall error

The magnitude of the deviation from a straight line between the endpoints of the transfer function.

differential nonlinearity

The maximum deviation of an analog-value change associated with a 1-bit code change (1 clock pulse) from its theoretical value of 1 LSB.

PARAMETER MEASUREMENT INFORMATION

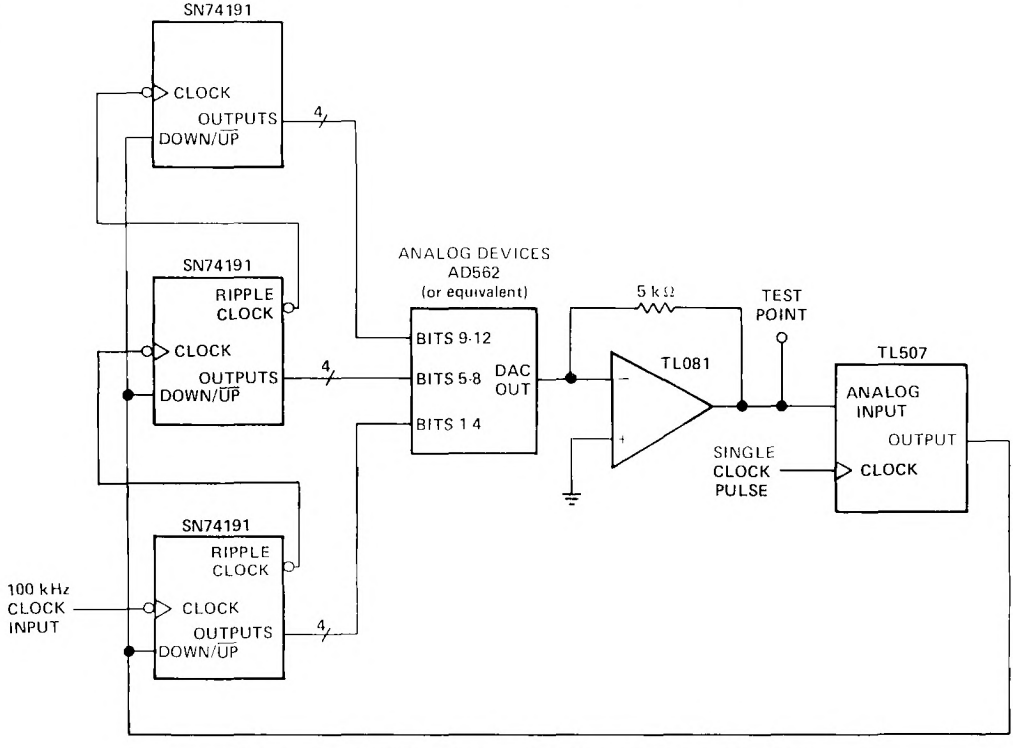


FIGURE 1. MONOTONICITY AND NONLINEARITY TEST CIRCUIT

PRINCIPLES OF OPERATION

The TL507 is a single-slope analog-to-digital converter. All single-slope converters are basically voltage-to-time or current-to-time converters. A study of the functional block diagram shows the versatility of the TL507.

An external clock signal is applied through a buffer to a negative-edge-triggered synchronous counter. Binary-weighted resistors from the counter are connected to an operational amplifier used as an adder. The operational amplifier generates a signal that ramps from $0.75 \cdot V_{CC1}$ down to $0.25 \cdot V_{CC1}$. Comparator 1 compares the ramp signal to the analog input signal. Comparator 2 functions as a fault defector. With the analog input voltage in the range $0.25 \cdot V_{CC1}$ to $0.75 \cdot V_{CC1}$, the duty cycle of the output signal is determined by the unknown analog input, as shown in Figure 2 and the Function Table.

For illustration, assume $V_{CC1} = 5.12$ V,

$$0.25 \cdot V_{CC1} = 1.28 \text{ V}$$

$$1 \text{ binary count} = \frac{(0.75 - 0.25)\, V_{CC1}}{128} = 20 \text{ mV}$$

$$0.75 \cdot V_{CC1} - 1 \text{ count} = 3.82 \text{ V}$$

The output is an open-collector n-p-n transistor capable of withstanding up to 18 V in the off state. The output is current limited to the 8- to 12-mA range; however, care must be taken to ensure that the output does not exceed 5.5 V in the on state.

The voltage regulator section allows operation from either an unregulated 8- to 18-V V_{CC2} source or a regulated 3.5- to 6-V V_{CC1} source. Regardless of which external power source is used, the internal circuitry operates at V_{CC1}. When operating from a V_{CC1} source, V_{CC2} may be connected to V_{CC1} or left open. When operating from a V_{CC2} source, V_{CC1} can be used as a reference voltage output.

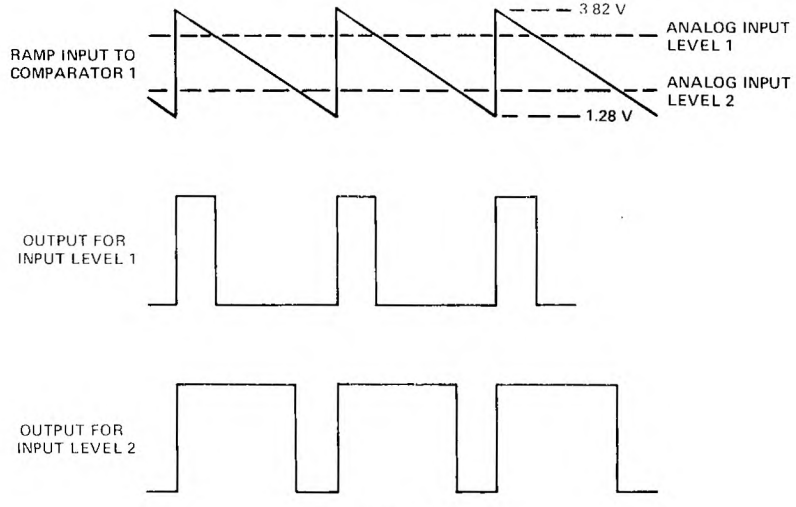


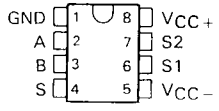
FIGURE 2

D2161, JUNE 1976 - REVISED OCTOBER 1986

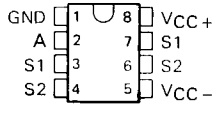
- Switch ± 10-V Analog Signals
- TTL Logic Capability
- 5- to 30-V Supply Ranges
- Low (100 Ω) On-State Resistance
- High (10^{11} Ω) Off-State Resistance
- 8-Pin Functions

JG OR P PACKAGE
(TOP VIEW)

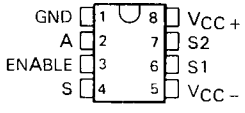
TL601



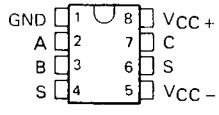
TL604



TL607



TL610



description

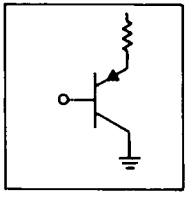
The TL601, TL604, TL607, and TL610 are a family of monolithic P-MOS analog switches that provide fast switching speeds with high r_{off}/r_{on} ratio and no offset voltage. The p-channel enhancement-type MOS switches accept analog signals up to ± 10 V and are controlled by TTL-compatible logic inputs. The monolithic structure is made possible by BI-MOS technology, which combines p-channel MOS with standard bipolar transistors.

These switches are particularly useful in military, industrial, and commercial applications such as data acquisition, multiplexers, A/D and D/A converters, MODEMS, sample-and-hold systems, signal multiplexing, integrators, programmable operational amplifiers, programmable voltage regulators, crosspoint switching networks, logic interface, and many other analog systems.

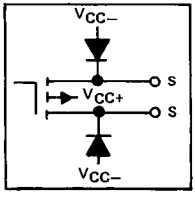
The TL601 is an SPDT switch with two logic control inputs. The TL604 is a dual complementary SPST switch with a single control input. The TL607 is an SPDT switch with one logic control input and one enable input. The TL610 is an SPST switch with three logic control inputs. The TL610 features a higher r_{off}/r_{on} ratio than the other members of the family.

The TL601M, TL604M, TL607M, and TL610M are characterized for operation over the full military temperature range of −55 °C to 125 °C, the TL601I, TL604I, TL607I, and TL610I are characterized for operation from −25 °C to 85 °C, and the TL601C, TL604C, TL607C, and TL610C are characterized for operation from 0 °C to 70 °C.

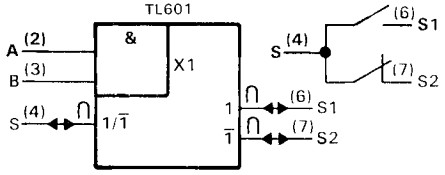
TYPICAL OF
ALL INPUTS



TYPICAL OF
ALL SWITCHES

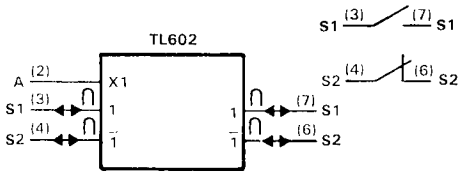


logic symbols† and switch diagrams



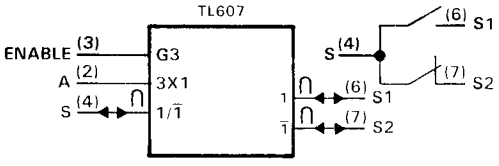
FUNCTION TABLE

LOGIC INPUTS		ANALOG SWITCH	
A	B	S1	S2
L	X	OFF (OPEN)	ON (CLOSED)
X	L	OFF (OPEN)	ON (CLOSED)
H	H	ON (CLOSED)	OFF (OPEN)



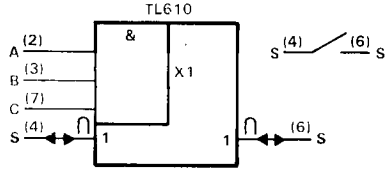
FUNCTION TABLE

LOGIC INPUT	ANALOG SWITCH	
A	S1	S2
H	ON (CLOSED)	OFF (OPEN)
L	OFF (OPEN)	ON (CLOSED)



FUNCTION TABLE

INPUTS		ANALOG SWITCH	
A	ENABLE	S1	S2
X	L	OFF (OPEN)	OFF (OPEN)
L	H	OFF (OPEN)	ON (CLOSED)
H	H	ON (CLOSED)	OFF (OPEN)

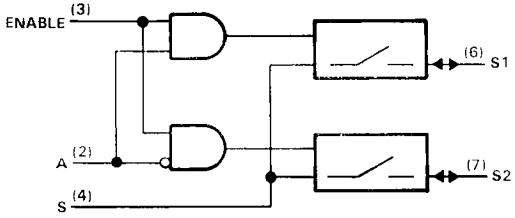


FUNCTION TABLE

INPUTS			ANALOG SWITCH
A	B	C	S
L	X	X	OFF (OPEN)
X	L	X	OFF (OPEN)
X	X	L	OFF (OPEN)
H	H	H	ON (CLOSED)

†These symbols are in accordance with ANSI/IEEE Std 91-1984.

TL607 logic diagram (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 30 V
Supply voltage, V_{CC-} . . . . . −30 V
V_{CC+} to V_{CC-} supply voltage differential . . . . . 35 V
Control input voltage . . . . . V_{CC+}
Switch off-state voltage . . . . . 30 V
Switch on-state current . . . . . 10 mA
Operating free-air temperature range: TL601M, TL604M, TL607M, TL610M . . . . −55°C to 125°C
TL601I, TL604I, TL607I, TL610I . . . . . −25°C to 85°C
TL601C, TL604C, TL607C, TL610C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature (1,6 mm) 1/16 inch from case for 60 seconds: JG package . . . . . 300°C
Lead temperature (1,6 mm) 1/16 inch from case for 10 seconds: P package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	TL601M, TL604M TL607M, TL610M			TL601I, TL604I TL607I, TL610I			TL601C, TL604C TL607C, TL610C			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+} (see Figure 1)	5	10	25	5	10	25	5	10	25	V
Supply voltage, V_{CC-} (see Figure 1)	−5	−20	−25	−5	−20	−25	−5	−20	−25	V
V_{CC+} to V_{CC-} supply voltage differential (see Figure 1)	15		30	15		30	15		30	V
High-level control input voltage, V_{IH}	2		5.5	2		5.5	2		5.5	V
Low-level control input voltage, V_{IL} All inputs			0.8			0.8			0.8	
Voltage at any analog switch (S) terminal	$V_{CC-}+8$		V_{CC+}	$V_{CC-}+8$		V_{CC+}	$V_{CC-}+8$		V_{CC+}	V
Switch on-state current			10			10			10	mA
Operating free-air temperature, T_A	−55		125	−25		85	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 10 V, V_{CC-} = −20 V, analog switch test current = 1 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TL6__M TL6__I MIN	TL6__M TL6__I TYP‡	TL6__M TL6__I MAX	TL6__C MIN	TL6__C TYP‡	TL6__C MAX	UNIT
I_{IH}	High-level input current	V_I = 5.5 V				0.5	10		0.5	10	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−50	−250		−50	−250	μA
I_{off}	Switch off-state current	$V_{I(sw)}$ = −10 V, See Note 2		T_A = 25°C		−400			−500		pA
				T_A = MAX†		−50	−100		−10	−20	nA
r_{on}	Switch on-state resistance	$V_{I(sw)}$ = 10 V, $I_{O(sw)}$ = 1 mA		TL601 TL604 TL607		55	100		75	200	Ω
				TL610		40	80		40	100	
		$V_{I(sw)}$ = 10 V, $I_{O(sw)}$ = −1 mA		TL601 TL604 TL607		220	400		220	600	
				TL610		120	300		120	400	
r_{off}	Switch off-state resistance					25			20		GΩ
C_{on}	Switch on-state input capacitance	$V_{I(sw)}$ = 0 V, f = 1 MHz				16			16		pF
C_{off}	Switch off-state input capacitance	$V_{I(sw)}$ = 0 V, f = 1 MHz				8			8		pF
I_{CC+}	Supply current from V_{CC+}	Logic input(s) at 5.5 V, All switch terminals open		TL601 TL604		5	10		5	10	mA
			Enable input high	TL607		5	10		5	10	
			Enable input low			3	5		3	5	
				TL610		5	10		5	10	
I_{CC-}	Supply current from V_{CC-}	Logic input(s) at 5.5 V, All switch terminals open		TL601 TL604		1.2	2.5		1.2	2.5	mA
			Enable input high	TL607		−2.5	−5		−2.5	−5	
			Enable input low			−0.05	−0.5		−0.05	−0.5	
				TL610		1.2	2.5		1.2	2.5	

†MAX is 125°C for M-suffix types, 85°C for I-suffix types, and 70°C for C-suffix types.
‡All typical values are at T_A = 25°C except for I_{off} at T_A = MAX.
NOTE 2: The other terminal of the switch under test is at V_{CC+} = 10 V.

switching characteristics, V_{CC+} = 10 V, V_{CC-} = −20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Switch turn-off time	R_L = 1 kΩ, C_L = 35 pF, See Figure 2		400	500	ns
t_{on}	Switch turn-on time			100	150	

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Figure 1 shows power supply boundary conditions for proper operation of the TL601 Series. The range of operation for supply V_{CC+} from +5 V to +25 V is shown on the vertical axis. The range of V_{CC-} from −5 V to −25 V is shown on the horizontal axis. A recommended 30-V maximum voltage differential from V_{CC+} to V_{CC-} governs the maximum V_{CC+} for a chosen V_{CC-} (or vice versa). A minimum recommended difference of 15 V from V_{CC+} to V_{CC-} and the boundaries shown in Figure 1 allow the designer to select the proper combinations of the two supplies.

The designer-selected V_{CC+} supply value for a chosen V_{CC-} supply value limits the maximum input voltage that can be applied to either switch terminal; that is, the input voltage should be between V_{CC-} +8 V and V_{CC+} to keep the on-state resistance within specified limits.

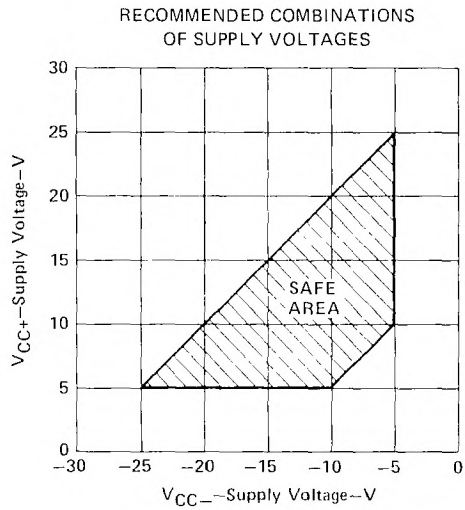
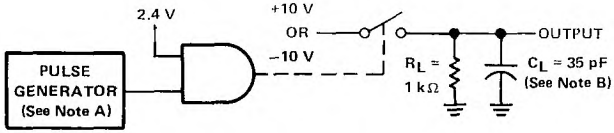
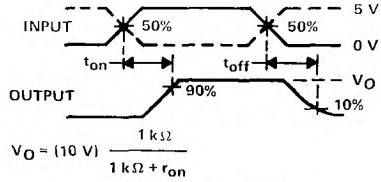


FIGURE 1

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics:
Z_{out} = 50 Ω, $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 500 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2

TYPICAL CHARACTERISTICS

M-SUFFIX DEVICES
I-SUFFIX DEVICES
SWITCH ON-STATE RESISTANCE
vs
SWITCH ANALOG VOLTAGE

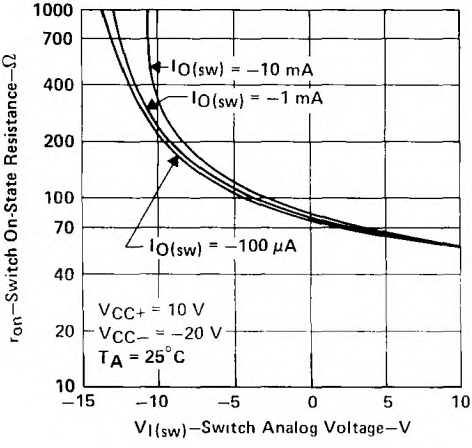


FIGURE 3

M-SUFFIX DEVICES
I-SUFFIX DEVICES
SWITCH ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

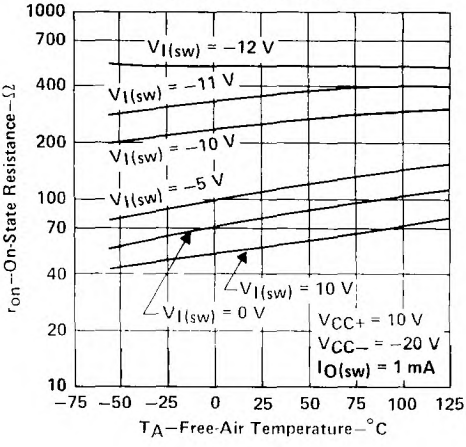


FIGURE 4

TEXAS INSTRUMENTS
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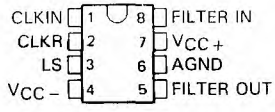
- **Low Clock-to-Cutoff-Frequency Ratio Error**
  TLC04/MF4A-50 . . . ±0.8%
  TLC14/MF4A-100 . . . ±1%
- **Filter Cutoff Frequency Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations Over Time and Temperature**
- **Cutoff Frequency Range from 0.1 Hz to 30 kHz, $V_{CC\pm}$ = ±2.5 V**
- **5-V to 12-V Operation**
- **Self Clocking or TTL-Compatible and CMOS-Compatible Clock Inputs**
- **Low Supply Voltage Sensitivity**
- **Designed to be Interchangeable with National MF4-50 and MF4-100**

D OR P PACKAGE
(TOP VIEW)



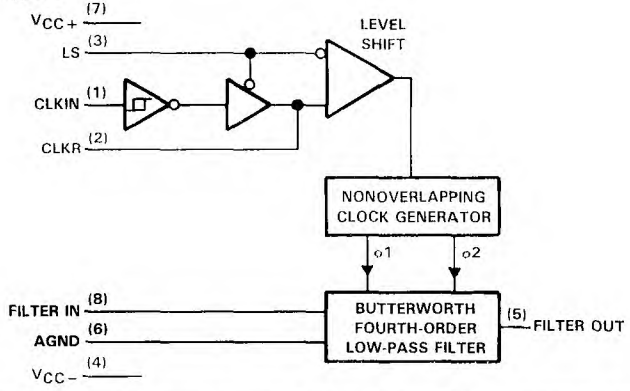
description

The TLC04/MF4A-50 and TLC14/MF4A-100 are monolithic Butterworth low-pass switched-capacitor filters. Each is designed as a low-cost, easy-to-use device providing accurate fourth-order low-pass filter functions in circuit design configurations.

Each filter features cutoff frequency stability that is dependent only on the external-clock frequency stability. The cutoff frequency is clock tunable and has a clock-to-cutoff frequency ratio of 50:1 with less than ±0.8% error for the TLC04/MF4A-50 and a clock-to-cutoff frequency ratio of 100:1 with less than ±1% error for the TLC14/MF4A-100. The input clock features self-clocking or TTL- or CMOS-compatible options in conjunction with the level shift (LS) pin.

The TLC04M/MF4A-50M and TLC14M/MF4A-100M are characterized over the full military temperature range of −55°C to 125°C. The TLC04I/MF4A-50I and TLC14I/MF4A-100I are characterized for operation from −40°C to 85°C. The TLC04C/MF4A-50C and TLC14C/MF4A-100C are characterized for operation from 0°C to 70°C.

functional block diagram



AVAILABLE OPTIONS

T_A	CLOCK-TO-CUTOFF FREQUENCY RATIO	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	50:1	TLC04CD/MF4A-50CD	TLC04CP/MF4A-50CP
	100:1	TLC14CD/MF4A-100CD	TLC14CP/MF4A-100CP
−40°C to 85°C	50:1	TLC04ID/MF4A-50ID	TLC04IP/MF4A-50IP
	100:1	TLC14ID/MF4A-100ID	TLC14IP/MF4A-100IP
−55°C to 125°C	50:1		TLC04MP/MF4A-50MP
	100:1		TLC14MP/MF4A-100MP

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC04CDR/MF4A-50CDR).

pin description

PIN NAME	NO.	I/O	DESCRIPTION
AGND	6	I	Analog Ground — The noninverting input to the operational amplifiers of the Butterworth fourth-order low-pass filter.
CLKIN	1	I	Clock In — The clock input terminal for CMOS-compatible clock or self-clocking options. For either option, the Level Shift (LS) terminal is at V_{CC-}. For self-clocking, a resistor is connected between the CLKIN and CLKR terminal pins and a capacitor is connected from the CLKIN terminal pin to ground.
CLKR	2	I	Clock R — The clock input for a TTL-compatible clock. For a TTL clock, the level shift pin is connected to mid-supply and the CLKIN pin may be left open, but it is recommended that it be connected to either V_{CC+} or V_{CC-}.
FILTER IN	8	I	Filter Input
FILTER OUT	5	O	Butterworth fourth-order low-pass Filter Output
LS	3	I	Level Shift — This terminal accommodates the various input clocking options. For CMOS-compatible clocks or self-clocking, the level-shift terminal is at V_{CC-} and for TTL-compatible clocks, the level-shift terminal is at mid-supply.
V_{CC+}	7	I	Positive supply voltage terminal
V_{CC-}	4	I	Negative supply voltage terminal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC\pm}$ (see Note 1) . . . . . ±7 V
Operating free-air temperature range: TLC04M/MF4A-50M, TLC14M/MF4A-100M −55°C to 125°C
TLC04I/MF4A-50I, TLC14I/MF4A-100I . . . . . −40°C to 85°C
TLC04C/MF4A-50C, TLC14C/MF4A-100C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

			TLC04/MF4A-50		TLC14/MF4A-100		UNIT
			MIN	MAX	MIN	MAX	
V_{CC+}	Positive supply voltage		2.25	6	2.25	6	V
V_{CC-}	Negative supply voltage		−2.25	−6	−2.25	−6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
f_{clock}	Clock frequency (see Note 2)	$V_{CC\pm}$ = ±2.5 V	5	1.5×10^6	5	1.5×10^6	Hz
		$V_{CC\pm}$ = ±5 V	5	2×10^6	5	2×10^6	
f_{co}	Cutoff frequency (see Note 3)		0.1	40×10^3	0.05	20×10^3	Hz
T_A	Operating free-air temperature	TLC04M/MF4A-50M, TLC14M/MF4A-100M	−55	125	−55	125	°C
		TLC04I/MF4A-50I, TLC14I/MF4A-100I	−40	85	−40	85	
		TLC04C/MF4A-50C, TLC14C/MF4A-100C	0	70	0	70	

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.
3. The cutoff frequency is defined as the frequency where the response is 3.01 dB less than the dc gain of the filter.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = −2.5 V, $f_{clock} \leq$ 250 kHz (unless otherwise noted)

filter section

PARAMETER			TEST CONDITIONS	TLC04/MF4A-50			TLC14/MF4A-100			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OO}	Output voltage offset				25			50		mV
V_{OM}	Peak output voltages	V_{OM+}	R_L = 10 kΩ	1.8	2		1.8	2		V
		V_{OM-}		−1.25	−1.7		−1.25	−1.7		
I_{OS}	Short-circuit output current	Source	T_A = 25°C, See Note 4		−0.5			−0.5		mA
		Sink			4			4		
I_{CC}	Supply current		f_{clock} = 250 kHz		1.2	2.25		1.2	2.25	mA

NOTE 4: I_{OS} (source current) is measured by forcing the output to its maximum positive voltage and then shorting the output to the negative supply (V_{CC-}) terminal. I_{OS} (sink current) is measured by forcing the output to its maximum negative voltage and then shorting the output to the positive supply (V_{CC+}) terminal.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 2.5 V, V_{CC-} = −2.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04/MF4A-50			TLC14/MF4A-100			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Maximum clock frequency, f_{max}	See Note 2		1.5	3		1.5	3		MHz
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	$f_{clock} \leq$ 250 kHz, T_A = 25°C		49.27	50.07	50.87	99	100	101	
Temperature coefficient of clock-to-cutoff frequency ratio	$f_{clock} \leq$ 250 kHz			±25			±25		ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 6 kHz	−7.9	−7.57	−7.1				dB
		f = 4.5 kHz	−1.7	−1.46	−1.3				
	f_{co} = 2.5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 3 kHz				−7.9	−7.42	−7.1	dB
		f = 2.25 kHz				−1.7	−1.51	−1.3	
Dynamic range (see Note 6)	T_A = 25°C			80			78		dB
Stop-band frequency attentuation at 2 f_{co}	$f_{clock} \leq$ 250 kHz		24	25		24	25		dB
DC voltage amplification	$f_{clock} \leq$ 250 kHz, RS ≤ 2 kΩ		−0.15	0	0.15	−0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			5			5		mV

† All typical values are at T_A = 25°C.

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.

5. The frequency responses at f are referenced to a dc gain of 0 dB.

6. The dynamic range is referenced to 1.06 V rms (1.5 V peak) where the wideband noise over a 30-kHz bandwidth is typically 106 μV rms for the TLC04/MF4A-50 and 135 μV rms for the TLC14/MF4A-100.

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electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, $f_{clock} \leq$ 250 kHz, (unless otherwise noted)

filter section

PARAMETER		TEST CONDITIONS	TLC04/MF4A-50 MIN	TLC04/MF4A-50 TYP†	TLC04/MF4A-50 MAX	TLC14/MF4A-100 MIN	TLC14/MF4A-100 TYP†	TLC14/MF4A-100 MAX	UNIT
V_{OO} Output voltage offset				150			200		mV
V_{OM} Peak output voltages	V_{OM+}	R_L = 10 kΩ	3.75	4.3		3.75	4.5		V
	V_{OM-}		−3.75	−4.1		−3.75	−4.1		
I_{OS} Short-circuit output current	Source	T_A = 25°C, See Note 4		−2			−2		mA
	Sink			5			5		
I_{CC} Supply current		f_{clock} = 250 kHz		1.8	3		1.8	3	mA
k_{SVS} Supply voltage sensitivity (see Figures 1 and 2)				−30			−30		dB

NOTE 4: I_{OS} (source current) is measured by forcing the output to its maximum positive voltage and then shorting the output to the negative supply (V_{CC-}) terminal. I_{OS} (sink current) is measured by forcing the output to its maximum negative voltage and then shorting the output to the positive supply (V_{CC+}) terminal.

clocking section

PARAMETER		TEST CONDITIONS‡		MIN	TYP†	MAX	UNIT
V_{T+} Positive-going input threshold voltage	CLKIN	V_{CC+} = 10 V, V_{CC-} = 0		6.1	7	8.9	V
		V_{CC+} = 5 V, V_{CC-} = 0		3.1	3.5	4.4	
V_{T-} Negative-going input threshold voltage		V_{CC+} = 10 V, V_{CC-} = 0		1.3	3	3.8	V
		V_{CC+} = 5 V, V_{CC-} = 0		0.6	1.5	1.9	
V_{hys} Hysteresis ($V_{T+} - V_{T-}$)		V_{CC+} = 10 V, V_{CC-} = 0		2.3	4	7.6	V
		V_{CC+} = 5 V, V_{CC-} = 0		1.2	2	3.8	
V_{OH} High-level output voltage	CLKR	V_{CC} = 10 V	I_O = −10 μA	9			V
		V_{CC} = 5 V		4.5			
V_{OL} Low level output voltage		V_{CC} = 10 V	I_O 10 μA			1	V
		V_{CC} = 5 V				0.5	
Input leakage current		V_{CC} = 10 V	Level Shift pin at mid-supply,			2	μA
		V_{CC} = 5 V	T_A = 25°C			2	
Output current		V_{CC} = 10 V	CLKR and CLKIN	−3	−7		mA
		V_{CC} = 5 V	shorted to V_{CC-}	−0.75	−2		
Output current		V_{CC} = 10 V	CLKR and CLKIN	3	7		mA
		V_{CC} = 5 V	shorted to V_{CC+}	0 75	2		

†All typical values are at T_A = 25°C.
‡$V_{CC} = V_{CC+} - V_{CC-}$.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC04/MF4A-50			TLC14/MF4A-100			UNIT
			MIN		MAX	MIN	TYP†	MAX	
Maximum clock frequency, f_{max} (see Note 2)			2	4		2	4		MHz
Clock-to-cutoff-frequency ratio (f_{clock}/f_{co})	$f_{clock} \le 250$ kHz, T_A = 25°C		49.58	49.98	50.38	99	100	101	
Temperature coefficient of clock-to-cutoff frequency ratio	$f_{clock} \le 250$ kHz			±15			±15		ppm/°C
Frequency response above and below cutoff frequency (see Note 5)	f_{co} = 5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 6 kHz	−7.9	−7.57	−7.1				dB
		f = 4.5 kHz	−1.7	−1.44	−1.3				
	f_{co} = 2.5 kHz, f_{clk} = 250 kHz, T_A = 25°C	f = 3 kHz				−7.9	−7.42	−7.1	dB
		f = 2.25 kHz				−1.7	−1.51	−1.3	
Dynamic range (see Note 7)	T_A = 25°C			86			84		dB
Stop-band frequency attenuation at 2 f_{co}	$f_{clock} \le 250$ kHz		24	25		24	25		dB
Voltage amplification	$f_{clock} \le 250$ kHz, RS ≤ 2 kΩ		−0.15	0	0.15	−0.15	0	0.15	dB
Peak-to-peak clock feedthrough voltage	T_A = 25°C			7			7		mV

† All typical values are at T_A = 25°C.

NOTES: 2. Above 250 kHz, the input clock duty cycle should be 50% to allow the operational amplifiers the maximum time to settle while processing analog samples.

5. The frequency responses at f are referenced to a dc gain of 0 dB.

7. The dynamic range is referenced to 2.82 V rms (4 V peak) where the wideband noise over a 30-kHz bandwidth is typically 142 μV rms for the TLC04/MF4A-50 and 178 μV rms for the TLC14/MF4A-100.

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TYPICAL CHARACTERISTICS

FILTER OUTPUT
vs
SUPPLY VOLTAGE V_{CC+} RIPPLE FREQUENCY

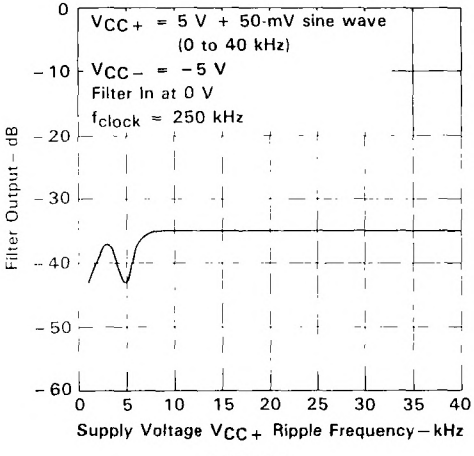

FIGURE 1

FILTER OUTPUT
vs
SUPPLY VOLTAGE V_{CC-} RIPPLE FREQUENCY

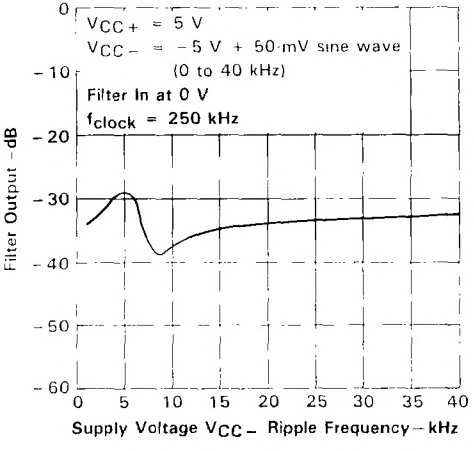

FIGURE 2

TYPICAL APPLICATION DATA

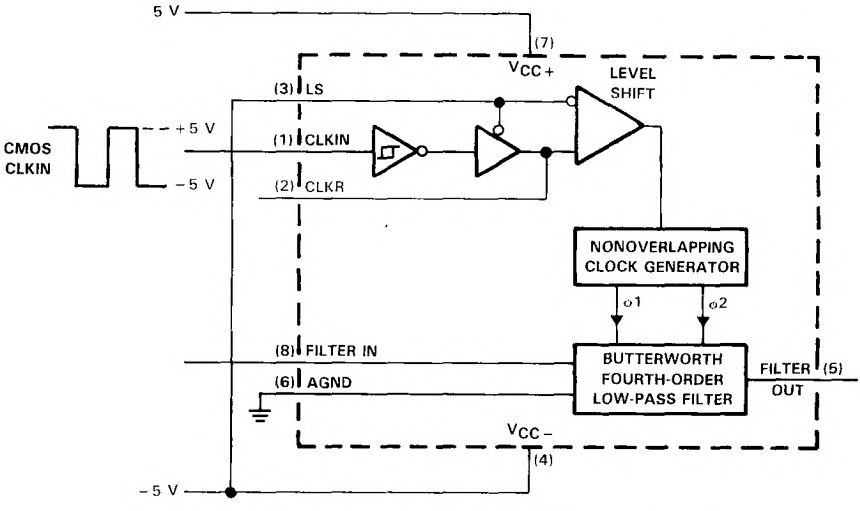

FIGURE 3. CMOS-CLOCK-DRIVEN, DUAL-SUPPLY OPERATION

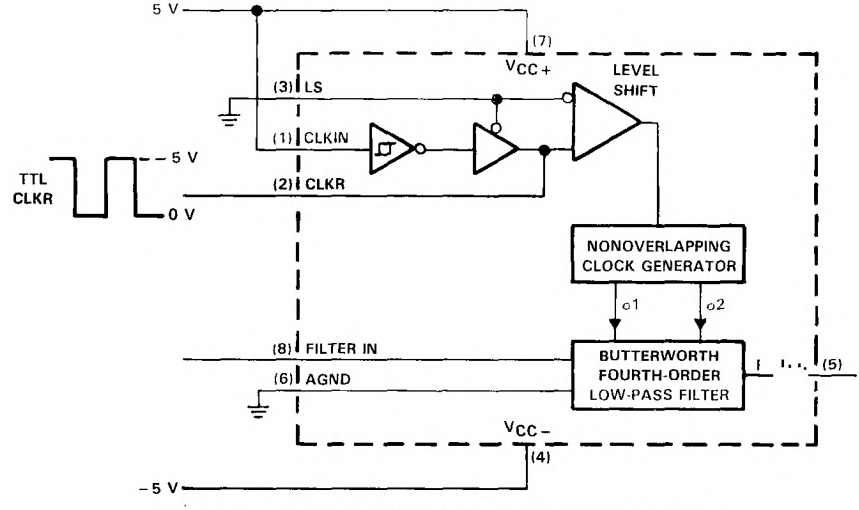

FIGURE 4. TTL-CLOCK-DRIVEN, DUAL-SUPPLY OPERATION

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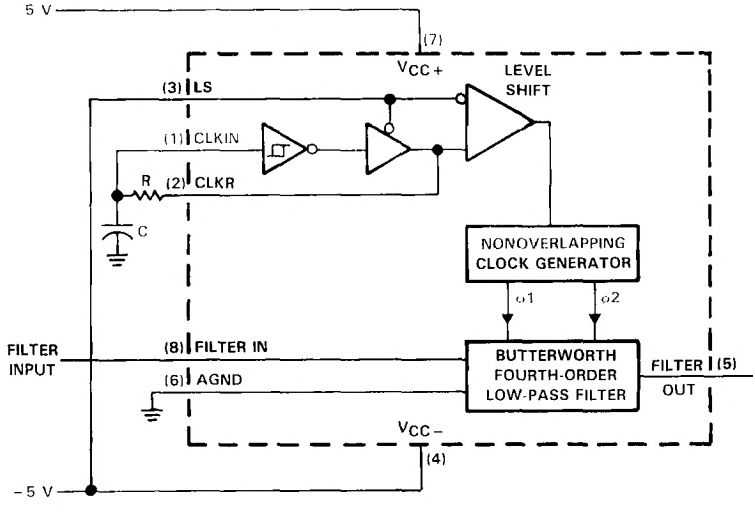
TYPICAL APPLICATION DATA



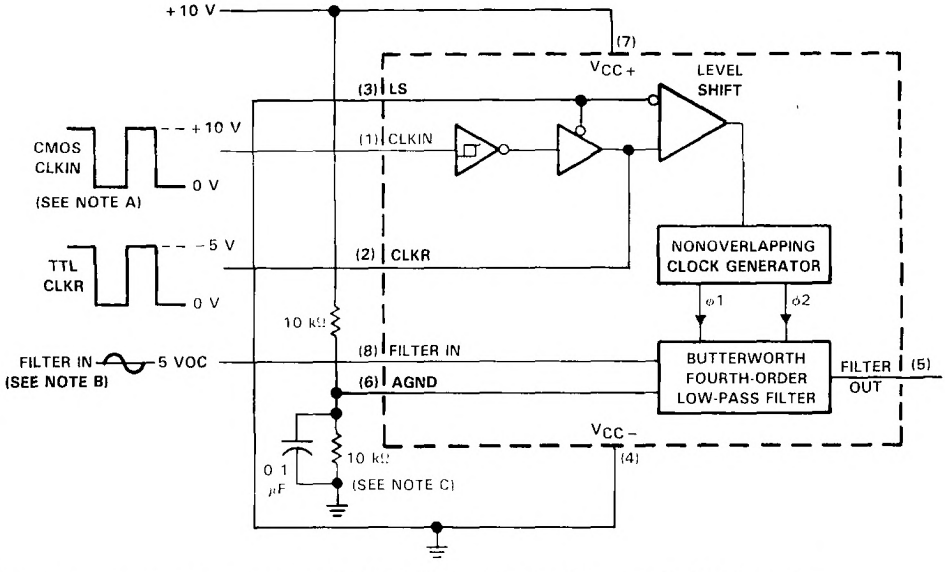
$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

For $V_{CC} = 10$ V,

$$f_{clock} = \frac{1}{1.69\ RC}$$

FIGURE 5. SELF-CLOCKING THROUGH SCHMITT-TRIGGER OSCILLATOR, DUAL-SUPPLY OPERATION

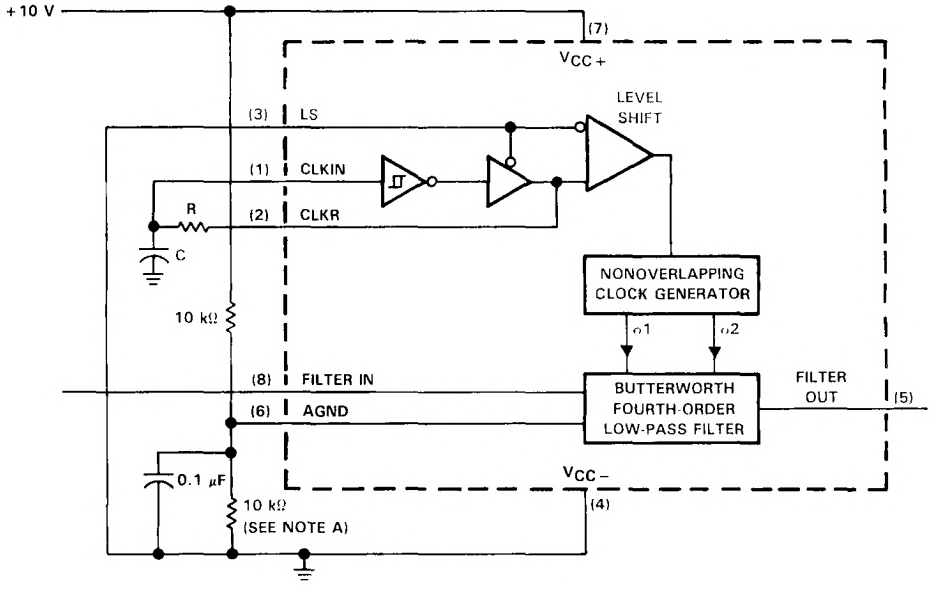
TYPICAL APPLICATION DATA



NOTES: A. The external clock used must be of CMOS level because the clock is input to a CMOS Schmitt trigger.
B. The Filter input signal should be dc-biased to mid-supply or ac-coupled to the terminal
C. The AGND terminal must be biased to mid supply

FIGURE 6. EXTERNAL-CLOCK-DRIVEN SINGLE-SUPPLY OPERATION

TYPICAL APPLICATION DATA



$$f_{clock} = \frac{1}{RC \times \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

For $V_{CC} = 10$ V,

$$f_{clock} = \frac{1}{1.69\ RC}$$

NOTE A: The AGND terminal must be biased to mid-supply.

FIGURE 7. SELF-CLOCKING THROUGH SCHMITT-TRIGGER OSCILLATOR, SINGLE-SUPPLY OPERATION

TYPICAL APPLICATION DATA

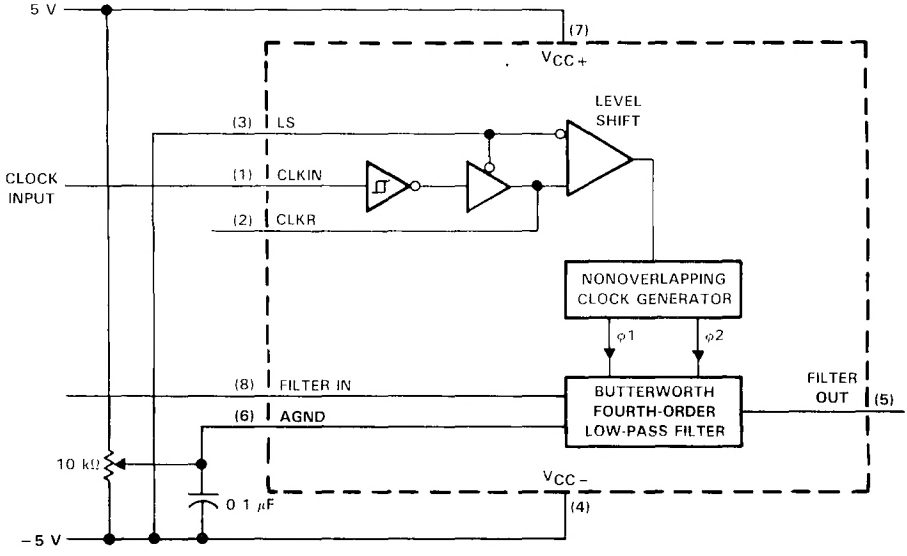
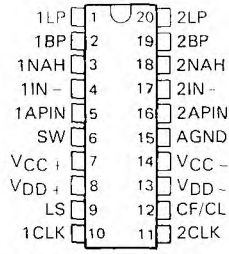


FIGURE 8. DC OFFSET ADJUSTMENT

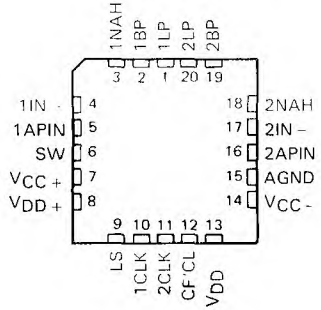
D2952, AUGUST 1986 – REVISED NOVEMBER 1988

- **Maximum Clock to Center-Frequency Ratio Error**
  TLC10 . . . ±0.6%
  TLC20 . . . ±1.5%
- **Filter Cutoff Frequency Stability Dependent Only on External-Clock Frequency Stability**
- **Minimum Filter Response Deviation Due to External Component Variations over Time and Temperature**
- **Critical-Frequency Times Q Factor Range Up to 200 kHz**
- **Critical-Frequency Operation Up to 30 kHz**
- **Designed to be Interchangeable with:**
  National MF10
  Maxim MF10
  Linear Technology LTC1060

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC10/MF10A and TLC20/MF10C are monolithic general-purpose switched-capacitor CMOS filters each containing two independent active-filter sections. Each device facilitates configuration of Butterworth, Bessel, Cauer, or Chebyshev filter design.

Filter features include cutoff frequency stability that is dependent only on the external clock frequency stability and minimal response deviation over time and temperature. Features also include a critical-frequency times filter quality (Q) factor range of up to 200 kHz.

With external clock and resistors, each filter section can be used independently to produce various second-order functions or both sections can be cascaded to produce fourth-order functions. For functions greater than fourth-order, ICs can be cascaded.

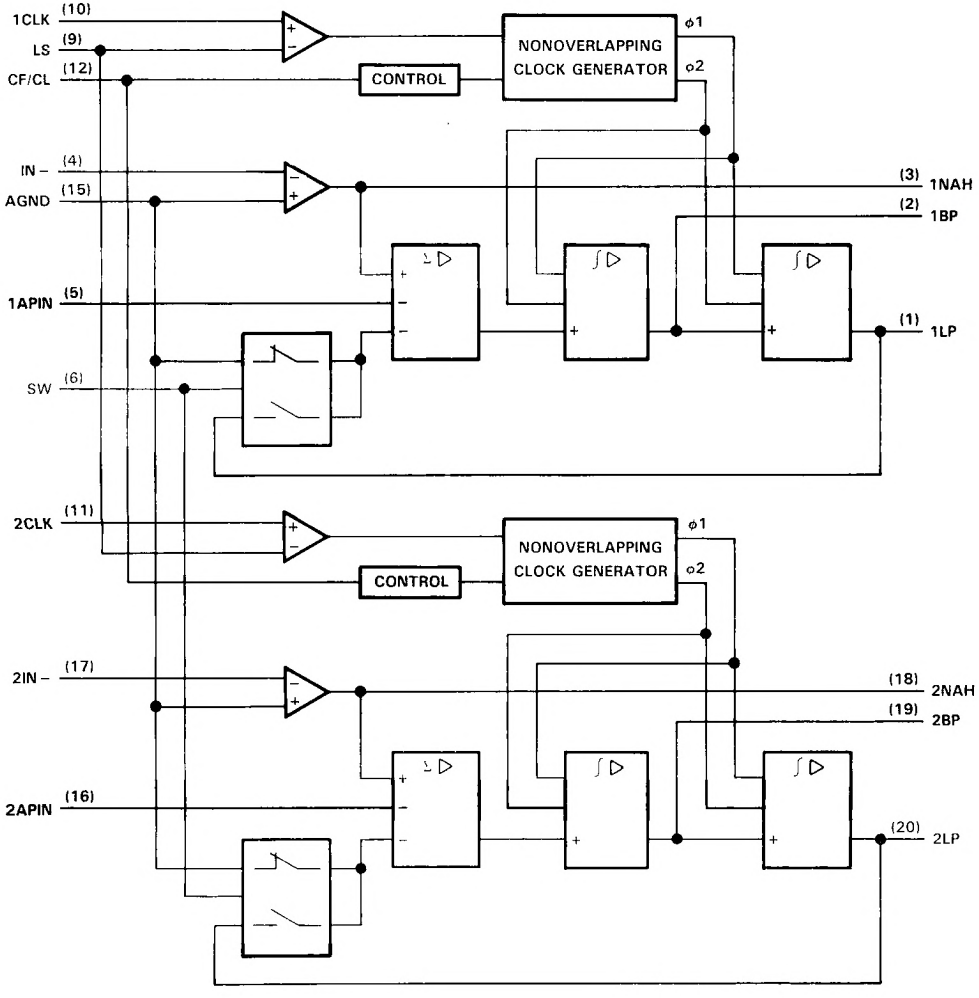
The TLC10/MF10A and TLC20/MF10C are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	MAX f_{clock}/fc ERROR	PACKAGE	
		CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	±0.6%	TLC10CFN or MF10ACFN	TLC10CN or MF10ACN
	±1.5%	TLC20CFN or MF10CCFN	TLC20CN or MF10CCN

PIN NAME	PIN NO.	I/O	DESCRIPTION
AGND	15	I	Analog Ground — The noninverting inputs to the input operational amplifiers of both filter sections. This terminal should be at ground for dual supplies or at mid-supply level for single-supply operation.
1APIN 2APIN	5 16	I	All-Pass Inputs — The all-pass input to the summing amplifier of each respective filter section used for all-pass filter applications in configuration modes 1a, 4, 5, and 6. This terminal should be driven from a source having an impedance of less than 1 kΩ. In all other modes, this terminal is grounded. See Typical Application Data.
1BP 2BP	2 19	O	Band-Pass Outputs — The band-pass output of each respective filter section provides the second-order band-pass filter functions.
CF/CL	12	I	Center Frequency/Current Limit — This input terminal provides the option to select the input-clock-to-center-frequency ratio of 50:1 or 100:1 or to limit the current of the IC. For a 50:1 ratio, the CF/CL terminal is set to V_{DD+}. For a 100:1 ratio, the CF/CL terminal is set to ground for dual supplies or to mid-supply level for single-supply operation. For current limiting, the CF/CL terminal is set to V_{DD-}. This aborts filtering and limits the IC current to 0.5 milliamperes.
1CLK 2CLK	10 11	I	Clock Inputs — The clock input to the two-phase nonoverlapping generator of each respective filter section is used to generate the center frequency of the complex pole pair second-order function. Both clocks should be of the same level (TTL or CMOS) and have duty cycles close to 50%, especially when clock frequencies (f_{clock}) greater than 200 kHz are used. At this duty cycle, the operational amplifiers have the maximum time to settle while processing analog samples.
1IN− 2IN−	4 17	I	Inverting Inputs — The inverting input side of the input operational amplifier whose output drives the summing amplifier of each respective filter section.
1LP 2LP	1 20	O	Low-Pass Outputs — The low-pass outputs of the second-order filters.
LS	9	I	Level Shift — This terminal accommodates various input clock levels of bipolar (CMOS) or unipolar (TTL or other clocks) to function with single or dual supplies. For CMOS (±5-volt) clocks, V_{DD-} or ground is applied to the LS terminal. For TTL and other clocks, ground is applied to the LS terminal.
1NAH 2NAH	3 18	O	Notch, All-Pass, or High-Pass Outputs — The output of each respective filter section can be used to provide either a second-order notch, all-pass, or high-pass output filter function, depending on circuit uration.
SW	6	I	Switch Input — This input terminal is used to control internal switches to connect either the A nput or the LP output to one of the inputs of the summing amplifier. The terminal controls both independent filter sections and places them in the same configuration simultaneously. If V_{CC-} is applied to the SW terminal, the AGND input terminal will be connected to one of the inputs of each summing amplifier. If V_{CC+} is applied to the SW terminal, the LP output will be connected to one of the inputs of the summing amplifier.
V_{CC+}	7		Analog positive supply voltage terminal
V_{CC-}	14		Analog negative supply voltage terminal
V_{DD+}	8		Digital positive supply voltage terminal
V_{DD-}	13		Digital negative supply voltage terminal

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Analog supply voltage, $V_{CC\pm}$ (see Note 1) . . . . . ±7 V
Digital supply voltage, $V_{DD\pm}$ . . . . . ±7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FN or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to the AGND terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, $V_{CC\pm}$, (see Note 2)	±4	±5	±6	V
Digital supply voltage, $V_{DD\pm}$, (see Note 2)	±4	±5	±6	V
Clock frequency, f_{clock} (see Note 3)	0.008		1.0	MHz
Operating free-air temperature, T_A	0		70	°C

NOTES: 2. A common supply voltage source should be used for the analog and digital supply voltages. Although each has separate terminals, they are connected together internally at the substrate. V_{CC+} and V_{DD+} can be connected together at the device terminals or at the supply voltage source. The same is true for V_{CC-} and V_{DD-}.
3. Both input clocks should be of the same level type (TTL or CMOS), and their duty cycles should be at 50% above 200 kHz to allow the operational amplifiers the maximum time to settle while processing analog samples.

electrical characteristics at $V_{CC\pm}$ = ±5 V, $V_{DD\pm}$ + = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TLC10/MF10A			TLC20/MF10C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OPP}	Maximum peak-to-peak output voltage swing		R_L = 3.5 kΩ at all outputs	±4	±4.1		±3.8	±3.9		V
I_{OS}	Short-circuit output current, Pins 3 and 18	Source	See Note 4		2			2		mA
		Sink			50			50		
I_{CC}	Supply current				8	10		8	10	mA

NOTE 4: The short-circuit output current for pins 1, 2, 19, and 20 will be typically the same as pins 3 and 18.

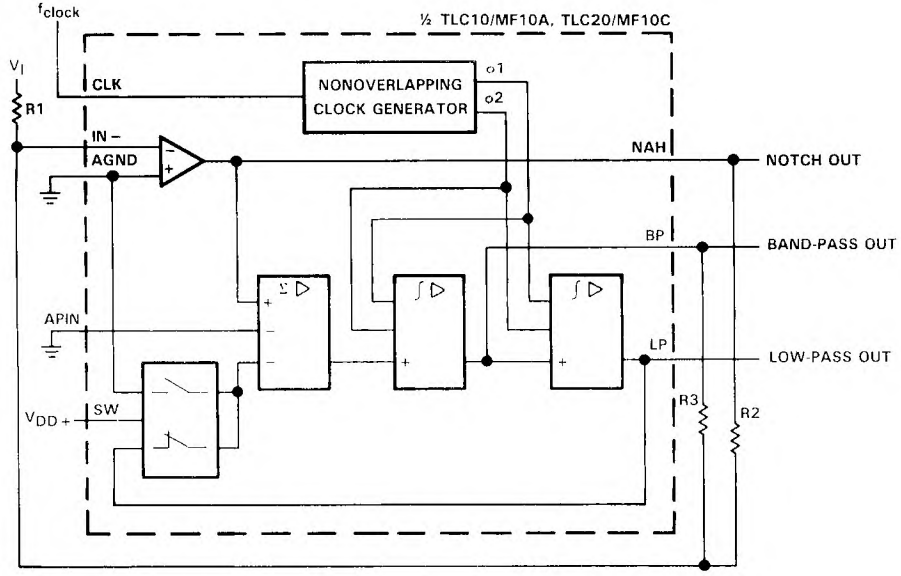
operating characteristics at $V_{CC\pm}$ = ±5 V, $V_{DD\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLC10/MF10A			TLC20/MF10C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Critical-frequency range	$f_0 \times Q \leq 200$ kHz		20	30		20	30		kHz
Maximum clock frequency, f_{clock}	See Note 3		1	1.5		1	1.5		MHz
Clock to center-frequency ratio	$f_0 \leq 5$ kHz, R3/R2 = 10, Mode 1, See Figure 1	Pin 12 at 5 V	49.64	49.94	50.24	49.24	49 94	50.64	
		Pin 12 at 0 V	98 75	99.35	99.95	97.86	99 35	100.84	
Temperature coefficient of center frequency	$f_0 \leq 5$ kHz, R3/R2 = 20, Mode 1, See Figure 1	Pin 12 at 5 V		±10			±10		ppm/°C
		Pin 12 at 0 V		±100			±100		
Filter Q (quality factor) deviation from 20	$f_0 \leq 5$ kHz, R3/R2 = 20, Mode 1, See Figure 1	Pin 12 at 5 V		±2%	±4%		±2%	±6%	
		Pin 12 at 0 V		±2%	±3%		±2%	±6%	
Temperature coefficient of measured filter Q	$f_0 \leq 5$ kHz, R3/R2 = 20, Mode 1			±500			±500		ppm/°C
Low-pass output deviation from unity gain	R1 = R2 = 10 kΩ, Mode 1, See Figure 1				±2%			±2%	
Crosstalk attenuation				60			60		dB
Clock feedthrough voltage				10			10		mV
Operational amplifier gain-bandwidth product				2.5			2.5		MHz
Operational amplifier slew rate				7			7		V/μs

TYPICAL APPLICATION DATA

modes of operation

The TLC10/MF10A and TLC20/MF10C are switched-capacitor (sampled-data) filters that closely approximate continuous filters. Each filter section is designed to approximate the response of a second-order variable filter. When the sampling frequency is much larger than the frequency band of interest, the sampled-data filter is a good approximation to its continuous time equivalent. In the case of the TLC10/MF10A and TLC20/MF10C, the ratio is about 50:1 or 100:1. To fully describe their transfer function, a time domain approach would be appropriate. Since this may appear cumbersome, the following application examples are based on the well known frequency domain. It should be noted that in order to obtain the actual filter response, the filter's response must be examined in the z-domain.

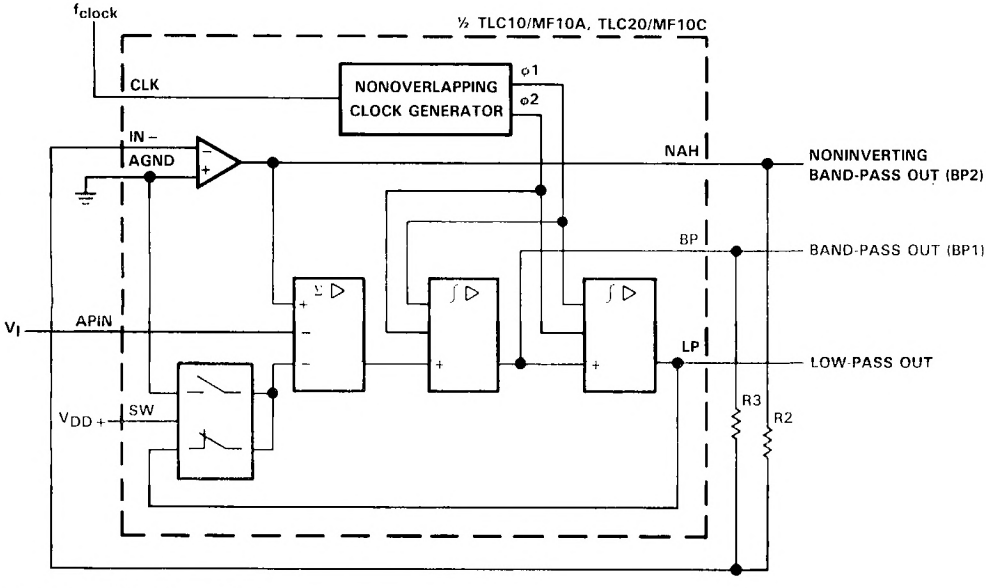


f_o = f_{clock} 100 or f_{clock} 50
f_{notch} = f_o
H_{OLP} = R2 R1 (as f → 0)
H_{OBP} = -R3 R1 (at f = f_o)
H_{ON} = notch gain { as f approaches 0 = R2 R1 ; as f approaches 0.5 f_{clock}
$Q = f_o/BW = R3/R2$

Circuit dynamics:
The following expressions determine the swing at each output as a function of the desired Q of the second-order function.
$H_{OLP} = H_{OBP}/Q$ or $H_{OLP} \times Q = H_{ON} \times Q$
H_{OLP} (peak) = $Q \times H_{OLP}$ (for high Qs)

FIGURE 1. MODE 1 FOR NOTCH, BAND-PASS, AND LOW-PASS OUTPUTS: $f_{notch} = f_o$

TYPICAL APPLICATION DATA

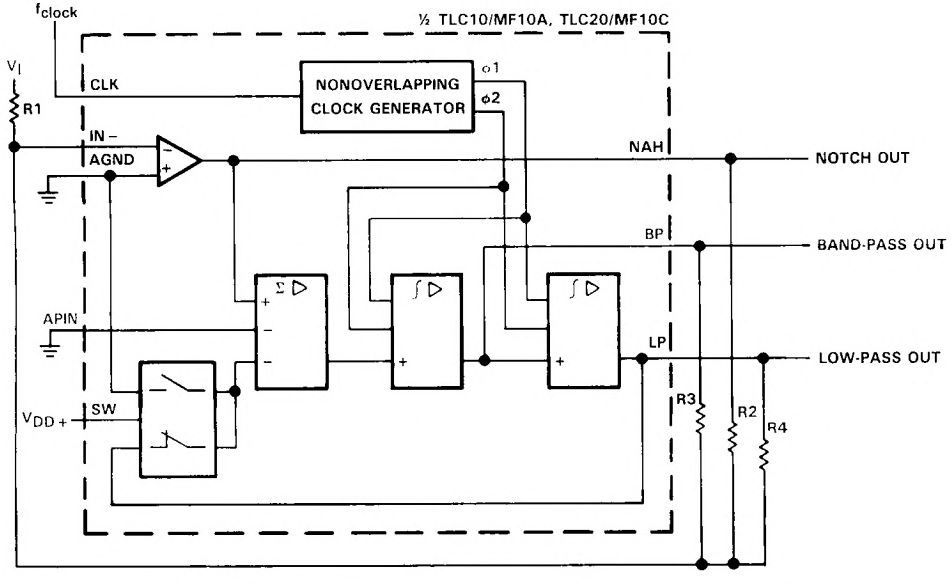


$f_o = f_{clock}/100$ or $f_{clock}/50$
Q R3/R2
H_{OLP} 1 H_{OLP} (peak) Q × H_{OLP} (for high Qs)
H_{OBP1} – R3/R2
H_{OBP2} 1 (noninverting)

Circuit dynamics
$H_{OBP1} = Q$

FIGURE 2. MODE 1a FOR NONINVERTING BAND-PASS AND LOW-PASS OUTPUTS

TYPICAL APPLICATION DATA



$f_o = f_{notch} \times \sqrt{R2/R4 + 1}$

$f_{notch} = f_{clock}/100$ or $f_{clock}/50$

$Q = \dfrac{\sqrt{R2/R4 + 1}}{R2/R3}$

H_{OLP} (as f approaches 0) $= \dfrac{-R2/R1}{R2/R4 + 1}$

H_{OBP} (at $f = f_o$) $= -R3/R1$

H_{ON1} (as f approaches 0) $= \dfrac{-R2/R1}{R2/R4 + 1}$

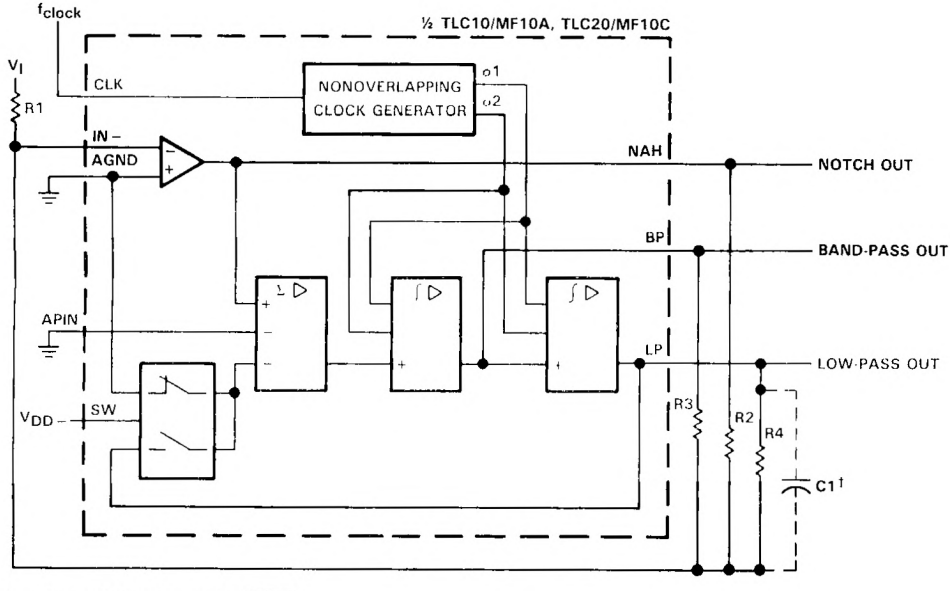
H_{ON2} (as f approaches 0.5 f_{clock}) $= -R2/R1$

Circuit dynamics:

$H_{OBP} = Q\sqrt{H_{OLP} \times H_{ON2}} = Q\sqrt{H_{ON1} \times H_{ON2}}$

FIGURE 3. MODE 2 FOR NOTCH 2, BAND-PASS, AND LOW-PASS OUTPUTS: $f_{notch} < f_o$

TYPICAL APPLICATION DATA



$f_o = (f_{clock}/100 \text{ or } f_{clock}/50)\sqrt{R2/R4}$

$Q = \sqrt{R2\ R4} \times R3\ R2$

H_{OHP} (as f approaches 0.5 f_{clock}) = $-R2/R1$

H_{OLP} (as f approaches 0) = $-R4/R1$

H_{OBP} (at f = f_o) = $R3\ R1$

Circuit dynamics:

$R2/R4 = H_{OHP}/H_{OLP}$; $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP}} \times Q$

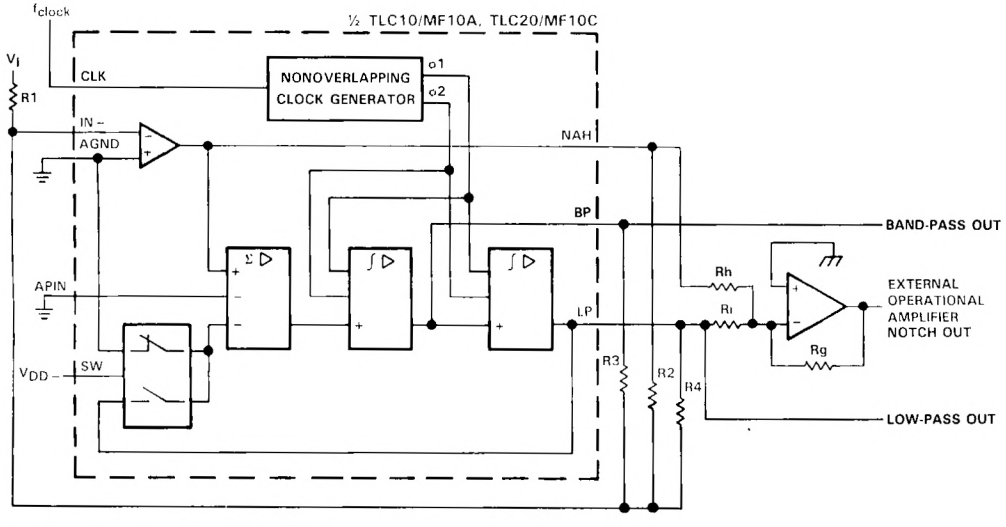
H_{OLP} (peak) = $Q \times H_{OLP}$ (for high Qs)

H_{OHP} (peak) = $Q \times H_{OHP}$ (for high Qs)

†In this mode, the feedback loop is closed around the input summing amplifier; the finite GBW product of this operational amplifier will cause a slight Q enhancement. If this is a problem, connect a low-value capacitor (10 pF to 100 pF) across R4 to provide some phase lead.

FIGURE 4. MODE 3 FOR HIGH-PASS, BAND-PASS, AND LOW-PASS OUTPUTS

TYPICAL APPLICATION DATA



$f_o = (f_{clock}/100 \text{ or } f_{clock}/50)\sqrt{R2/R4}$

$Q = \sqrt{R2/R4} \times R3/R2$

$H_{OHP} = R2/R1$

$H_{OBP} = R3/R1$

$H_{OLP} = R4/R1$

$f_{notch} = (f_{clock}/100 \text{ or } f_{clock}/50)\sqrt{Rh/Ri}$

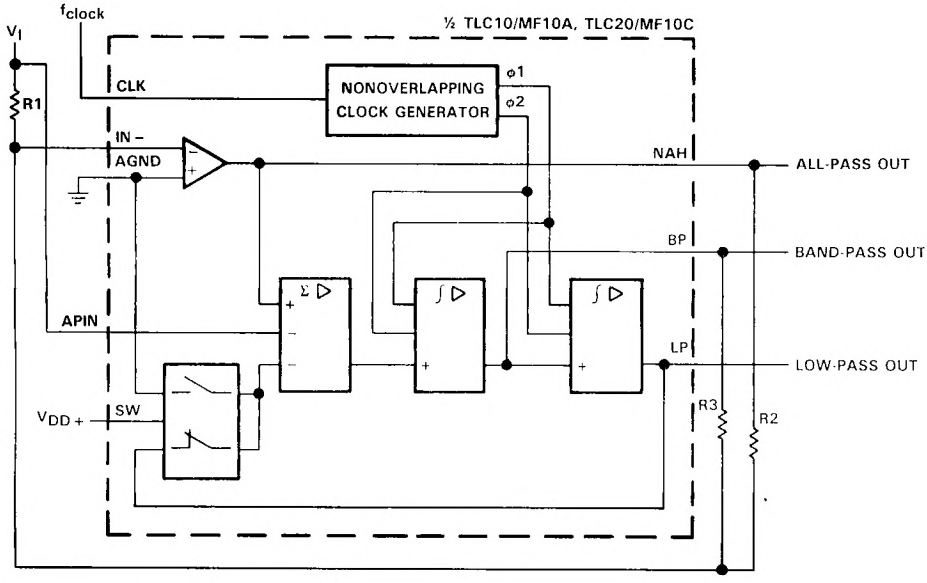
H_{ON} (at $f = f_o$) $= Q\,(Rg/Ri \times H_{OLP} - Rg/Rh \times HOHP)$

H_{ON1} (as f approaches 0) $= Rg/Ri \times H_{OLP}$

H_{ON2} (as f approaches 0.5 f_{clock}) $= -Rg/Rh \times H_{OHP}$

FIGURE 5. MODE 3a FOR HIGH-PASS, BAND-PASS, LOW-PASS, AND NOTCH OUTPUTS WITH EXTERNAL OPERATIONAL AMPLIFIER

TYPICAL APPLICATION DATA



f_o $f_{clock}/100$ or f_{clock} 50
f_z f_o†
Q f_o BW = R3/R2
Q_z = R3/R1
H_{OAP} (at $0 \le f \le 0.5\ f_{clock}$) = −R2/R1 = −1
(for AP output R1 = R2)
H_{OLP} (as f approaches 0) = −(R2/R1 + 1) = −2
H_{OBP} (at $f = f_o$) = −R3/R2 (R2/R1 + 1) = −2 (R3/R2)

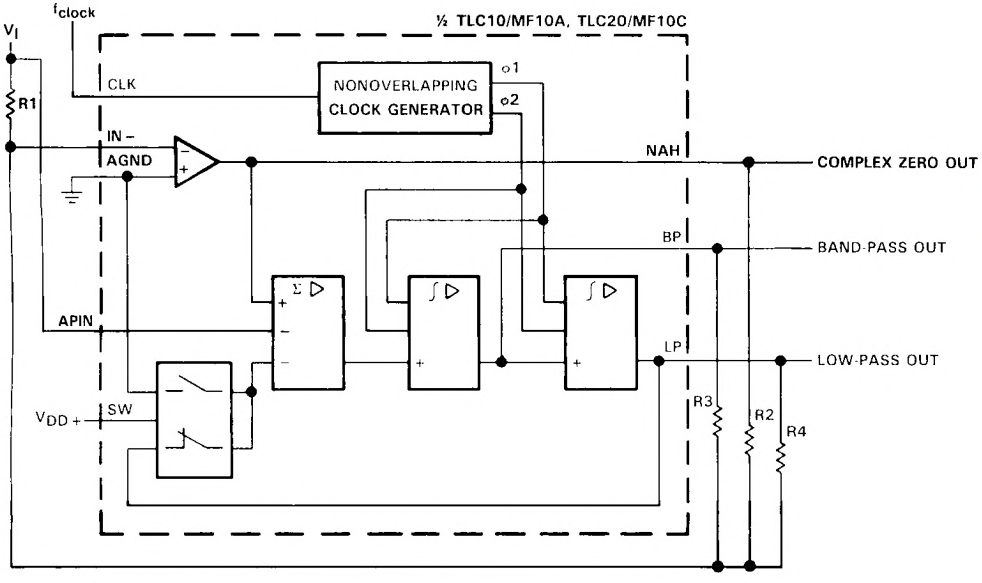
Circuit dynamics

H_{OBP} H_{OLP} > Q ((H_{OAP} 1) Q

†Due to the sampled-data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4-dB peaking around f_o of the all-pass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

FIGURE 6. MODE 4 FOR ALL-PASS, BAND-PASS, AND LOW-PASS OUTPUTS

TYPICAL APPLICATION DATA



$f_o = \sqrt{R2/R4 + 1} \times (f_{clock}/100 \text{ or } f_{clock}/50)$

$f_z = \sqrt{1 - R1/R4} \times (f_{clock}/100 \text{ or } f_{clock}/50)$

$Q = \sqrt{R2\,R4 - 1} \times R3\,R2$

$Q_z = \sqrt{1 - R1/R4} \times R3/R1$

H_{OZ1} (as f approaches 0) = R2 (R4 – R1)/R1 (R2 + R4)

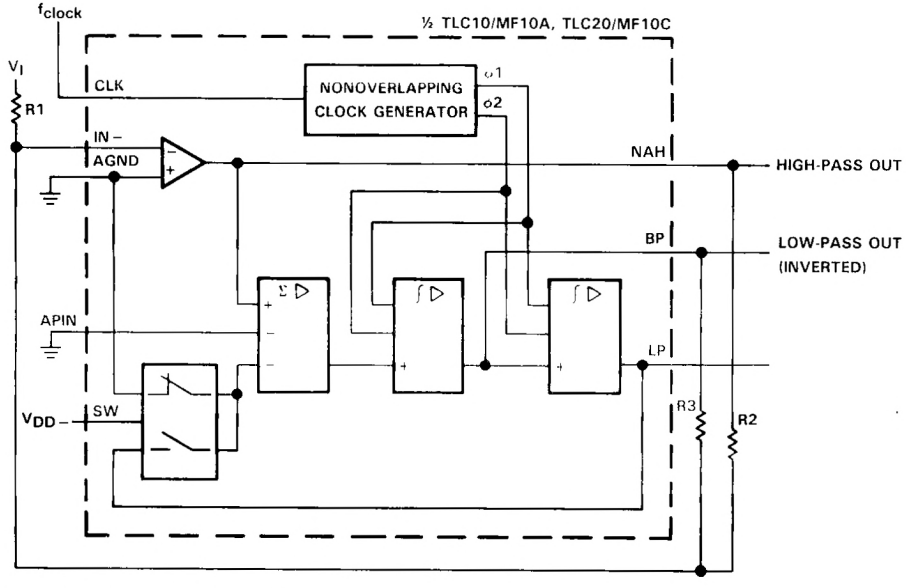
H_{OZ2} (as f approaches 0.5 f_{clock}) = R2/R1

$H_{OBP} = (R2/R1 + 1) \times R3/R2$

$H_{OLP} = (R2 + R1)/(R2 + R4) \times R4/R1$

FIGURE 7. MODE 5 FOR NUMERATOR COMPLEX ZEROS, BAND-PASS, AND LOW-PASS OUTPUTS

TYPICAL APPLICATION DATA



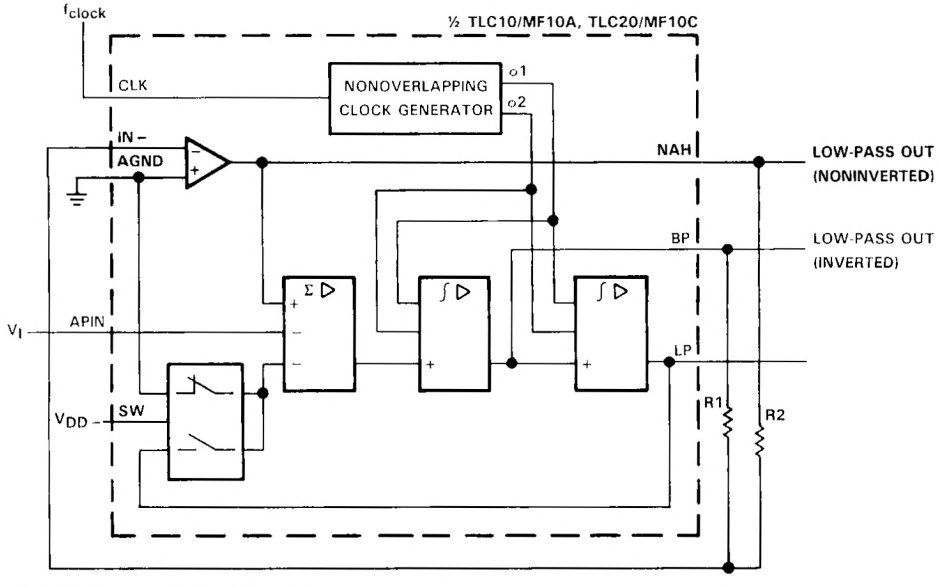
f_c = R2/R3 (f_{clock}/100 or f_{clock}/50)

H_{OLP} R3/R1

H_{OHP} R2/R1

FIGURE 8. MODE 6 FOR SINGLE-POLE HIGH-PASS AND LOW-PASS OUTPUT

TYPICAL APPLICATION DATA



f_c = R2/R3 × (f_{clock}/100 or f_{clock}/50)
H_{OLP1} = 1 (noninverting)
H_{OLP2} = R3 R2

FIGURE 9. MODE 6a FOR SINGLE-POLE LOW-PASS OUTPUT (INVERTED AND NONINVERTED)

TYPICAL APPLICATION DATA

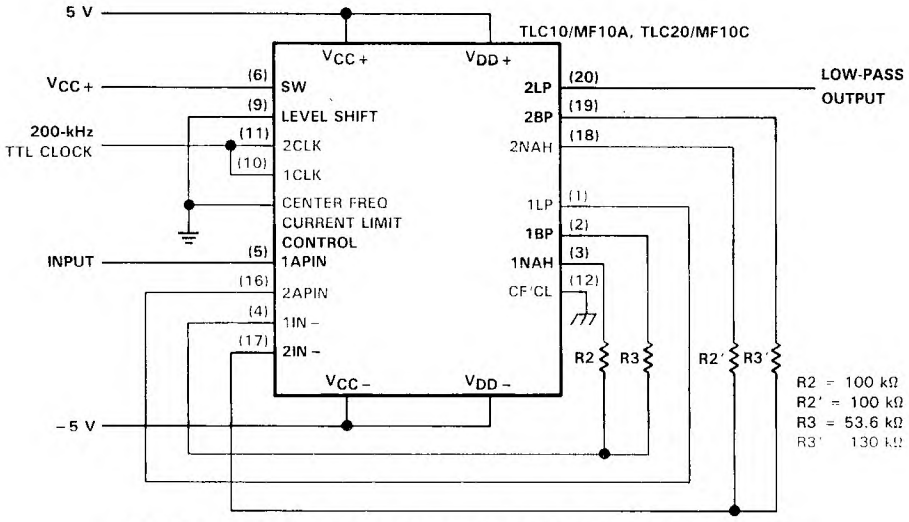
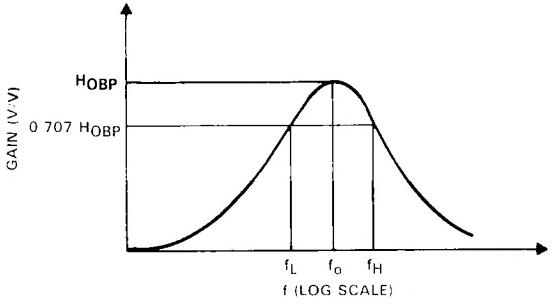


FIGURE 10. FOURTH-ORDER 2-kHz LOW-PASS BUTTERWORTH FILTER

filter terminology

f_c	The cutoff frequency of the low-pass or high-pass filter output
f_{clock}	The input clock frequency to the device
f_{notch}	The notch frequency of the notch output
f_o	The center frequency of the complex pole pair second-order function
f_z	The center frequency of the complex zero pair
H_{OBP}	The band-pass output voltage gain (V/V) at the band-pass center frequency
H_{OHP}	The high-pass output voltage gain (V/V) as the frequency approaches 0.5 f_{clock}
H_{OLP}	The low-pass output voltage gain (V/V) as the frequency approaches 0
H_{ON}	The notch output voltage gain (V/V) at the notch frequency
H_{ON1}	The low-side notch output voltage gain as the frequency approaches 0
H_{ON2}	The high-side notch output voltage gain as the frequency approaches 0.5 f_{clock}
H_{OZ1}	Gain at complex zero output (as $f \rightarrow 0$ Hz)
H_{OZ2}	Gain at complex zero output (as f approaches 0.5 f_{clock})
Q	The quality factor of the complex pole pair second-order function. Q is the ratio of f_o to the 3-dB bandwidth of the band-pass output. The value of Q also affects the possible peaking of the low-pass and high-pass outputs.
Q_z	The quality factor of the complex zero pair, if such a complex pair exists. This parameter is used when an all-pass filter output is desired.

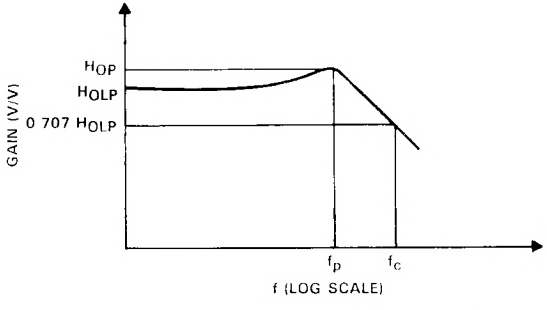


$$Q = \frac{f_o}{f_H - f_L} \; ; \; f_o = \sqrt{f_L f_H}$$

$$f_L = f_o \left(\frac{1}{2Q} - \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

$$f_H = f_o \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

FIGURE 11. BAND-PASS OUTPUT

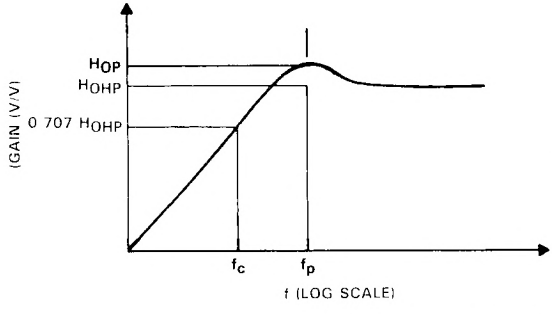


$$f_c = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_o \sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 12. LOW-PASS OUTPUT

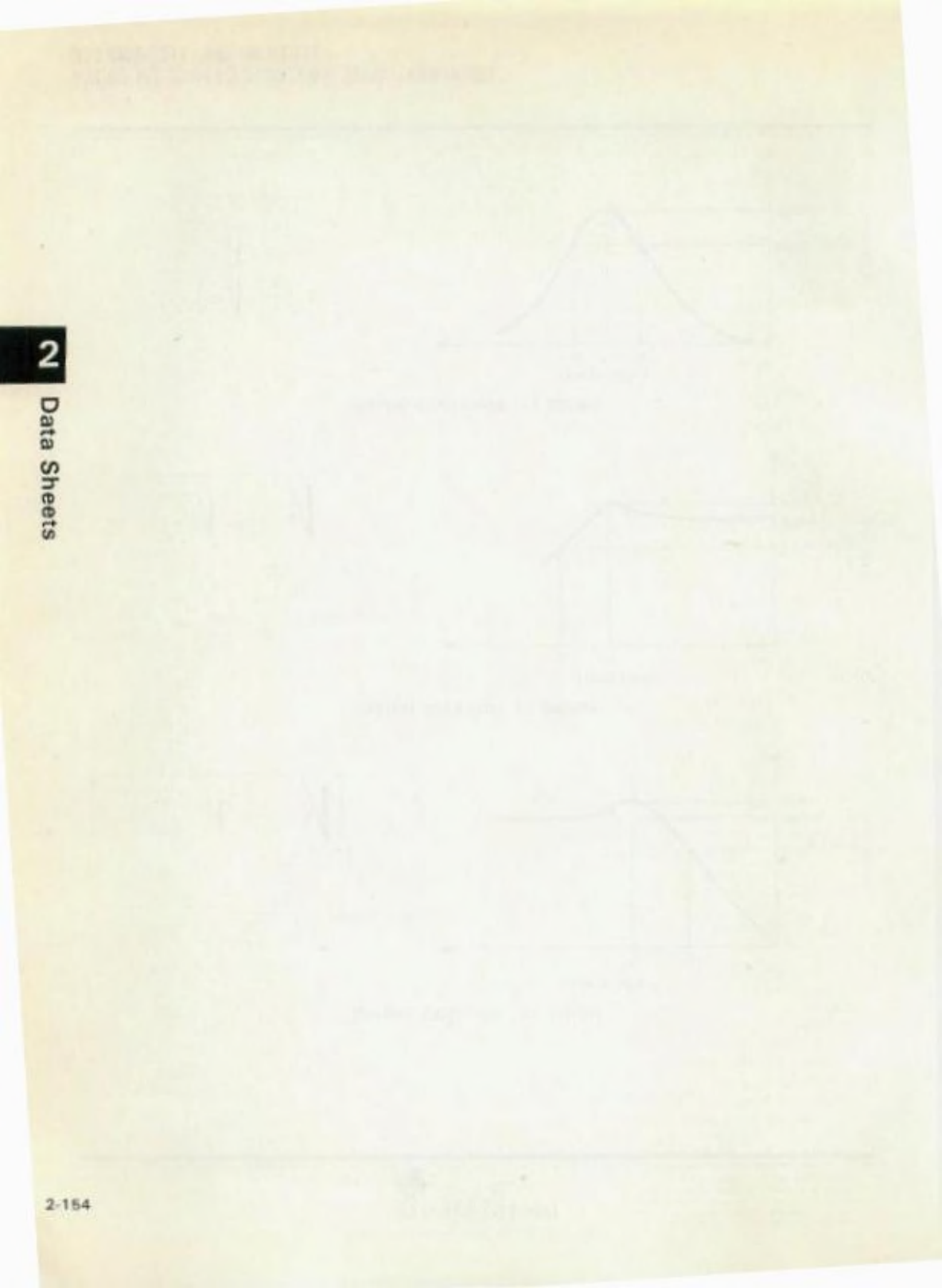


$$f_c = f_o \cdot \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}} \right]^{-1}$$

$$f_p = f_o \cdot \left[\sqrt{1 - \frac{1}{2Q^2}} \right]^{-1}$$

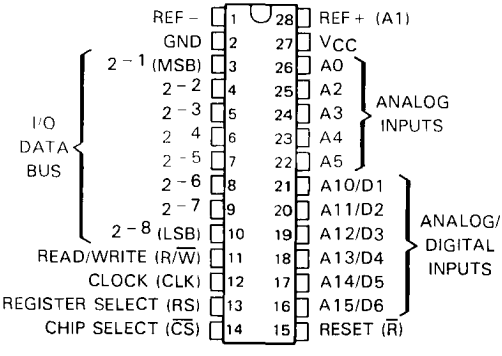
$$H_{OP} = H_{OHP} \cdot \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 13. HIGH-PASS OUTPUT

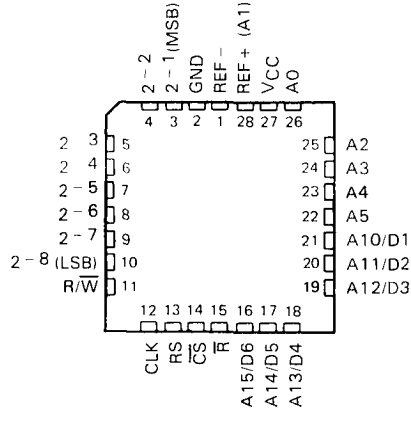


- LinCMOS™ Technology
- 8-Bit Resolution
- Total Unadjusted Error . . . ±0.5 LSB Max
- Ratiometric Conversion
- Access Plus Conversion Time:
  TLC532A . . . 15 μs Max
  TLC533A . . . 30 μs Max
- 3-State, Bidirectional I/O Data Bus
- 5 Analog and 6 Dual-Purpose Inputs
- On-Chip 12-Channel Analog Multiplexer
- Three On-Chip 16-Bit Data Registers
- Software Compatible with Larger TL530 and TL531 (21-Input Versions)
- On-Chip Sample-and-Hold Circuit
- Single 5-V Supply Operation
- Low Power Consumption . . . 6.5 mW Typ
- Improved Direct Replacements for Texas Instruments TL532 and TL533, National Semiconductor ADC0829, and Motorola MC14442

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC532A and TLC533A are monolithic LinCMOS™ peripheral integrated circuits each designed to interface a microprocessor for analog data acquisition. These devices are complete peripheral data acquisition systems on a single chip and can convert analog signals to digital data from up to 11 external analog terminals. Each device operates from a single 5-V supply and contains a 12-channel analog multiplexer, an 8-bit ratiometric analog-to-digital (A/D) converter, a sample-and-hold, three 16-bit registers, and microprocessor-compatible control circuitry. Additional features include a built-in self-test, six multipurpose (analog or digital) inputs, five external analog inputs, and an 8-pin input/output (I/O) data port. The three on-chip data registers store the control data, the conversion results, and the input digital data that can be accesssed via the microprocessor data bus in two 8-bit bytes (most-significant byte first). In this manner, a microprocessor can access up to 11 external analog inputs or 6 digital signals and the positive reference voltage that may be used for self-test.

FUNCTION TABLE

R/W	RS	CS	R	CLK	DESCRIPTION
X	X	X	L†		Reset
L	H	L	H	↓	Write bus data to control register
H	L	L	H	↑	Read data from analog conversion register
H	H	L	H	↑	Read data from ditigal data register
X	X	H	H	X	No response

H = High-level, L = Low-level, X = Irrelevant
↓ = High-to-low transition, ↑ = Low-to-high transition
†For proper operation, Reset must be low for at least three clock cycles

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description (continued)

The A/D conversion uses the successive-approximation technique and switched-capacitor circuitry. This method eliminates the possibility of missing codes, nonmonotonicity, and a need for zero or full-scale adjustment. Any one of 11 analog inputs (or self-test) can be converted to an 8-bit digital word and stored within 10 μs (TLC532A) or 20 μs (TLC533A) after instructions from the microprocessor are recognized. The on-chip sample-and-hold automatically minimizes errors due to noise on the analog inputs. Furthermore, differential high-impedance reference inputs are available to help isolate the analog circuitry from the logic and supply noises while easing ratiometric conversion and scaling.

The TLC532AM and TLC533AM are available in both the N and FN plastic packages and are characterized for operation from $-55\,^{\circ}C$ to $125\,^{\circ}C$. The TLC532AI and TLC533AI are characterized for operation from $-40\,^{\circ}C$ to $85\,^{\circ}C$.

functional description

The TLC532A and TLC533A provide direct interface to a microprocessor-based system. Control of the TLC532A and TLC533A is handled via the 8-line TTL-compatible 3-state data bus, the three control inputs (Read/Write, Register Select, and Chip Select), and the Clock input. Each device contains three 16-bit internal registers — the control register, the analog conversion data register, and the digital data register.

A high level at the Read/Write input and a low level at the Chip Select input set the device to output data on the 8-line data bus for the processor to read. A low level at the Read/Write input and a low level at the Chip Select input set the device to receive instructions into the internal control register on the 8-line data bus from the processor. When the device is in the read mode and the Register Select input is low, the processor reads the data contained in the analog conversion data register. However, when the Register Select input is high, the processor reads the data contained in the digital data register.

The control register is a write-only register into which the microprocessor writes command instructions for the device to start A/D conversion and to select the analog channel to be converted. The analog conversion data register is a read-only register that contains the current converter status and most recent conversion results. The digital data register is also a read-only register that holds the digital input logic levels from the six dual-purpose inputs.

Internally each device contains a byte pointer that selects the appropriate byte during two cycles of the Clock input in a normal 16-bit microprocessor instruction. The internal pointer automatically points to the most significant (MS) byte after the first complete clock cycle any time that the Chip Select is at the high level for at least one clock cycle. The device treats the next signal on the 8-line data bus as the MS byte. A low level at the Chip Select input activates the inputs and outputs and an internal function decoder. However, no data is transferred until the Clock goes high. The internal byte pointer first points to the MS byte of the selected register during the first clock cycle. After the first clock cycle in which the MS byte is accessed, the internal pointer switches to the LS byte and remains there for as long as Chip Select is low. The MS byte of any register may be accessed by either an 8-bit or a 16-bit microprocessor instruction; however, the LS byte may only be accessed by a 16-bit microprocessor instruction.

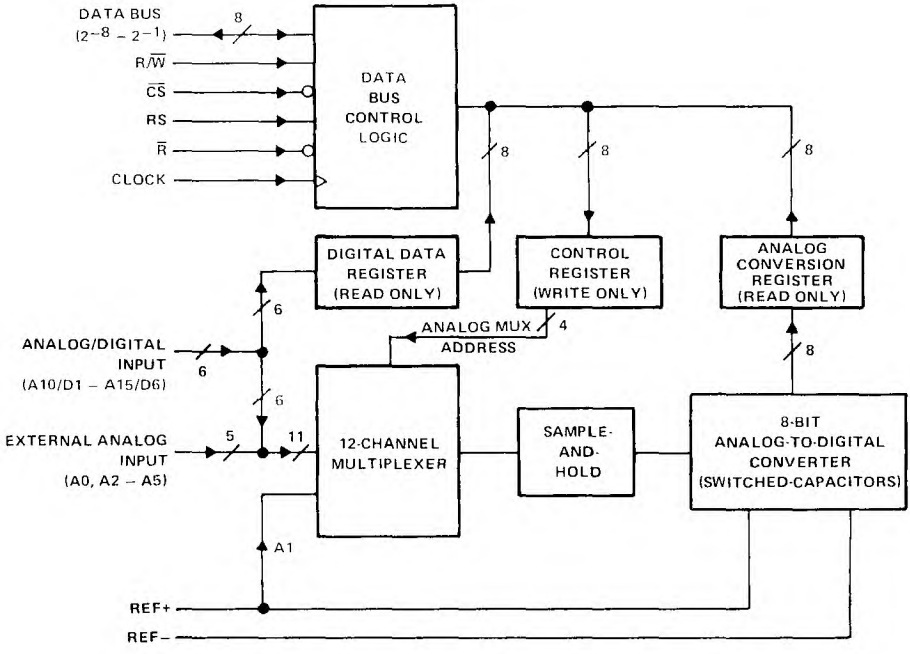
Normally, a 2-byte word is written or read from the controlling processor, but a single byte can be read by the processor by manipulating the Chip Select input. This can be used to read conversion status from the analog conversion data register or the digital multipurpose input levels from the digital data register. The format and content of each 2-byte word is shown in Figures 1 through 3.

functional description (continued)

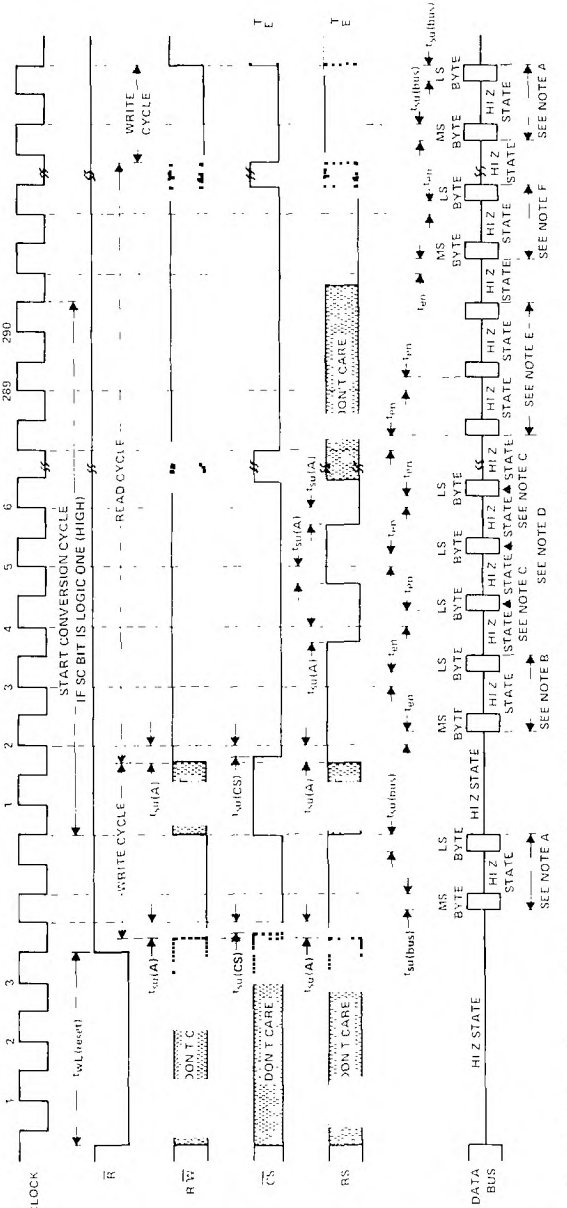
A conversion cycle starts after a 2-byte instruction is written to the control register and the start conversion (SC) bit is a logic high. This 2-byte instruction also selects the input analog channel to be converted. The status (EOC) bit in the analog conversion data register is reset, and it remains reset until the conversion is complete, at which time the status bit is set again. After conversion, the results are loaded into the analog conversion data register. These results remain in the analog conversion data register until the next conversion cycle is complete. If a new conversion command is entered into the control register while the conversion cycle is in progress, the on-going conversion is aborted and a new channel acquisition cycle begins immediately.

The Reset input allows the device to be externally forced to a known state. When a low level is applied to the Reset input for a minimum of three clock periods, the start conversion bit is cleared. The A/D converter is then idled and all the outputs are placed in the high-impedance off-state. However, the content of the analog conversion data register is not affected by the Reset input going to a low level.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

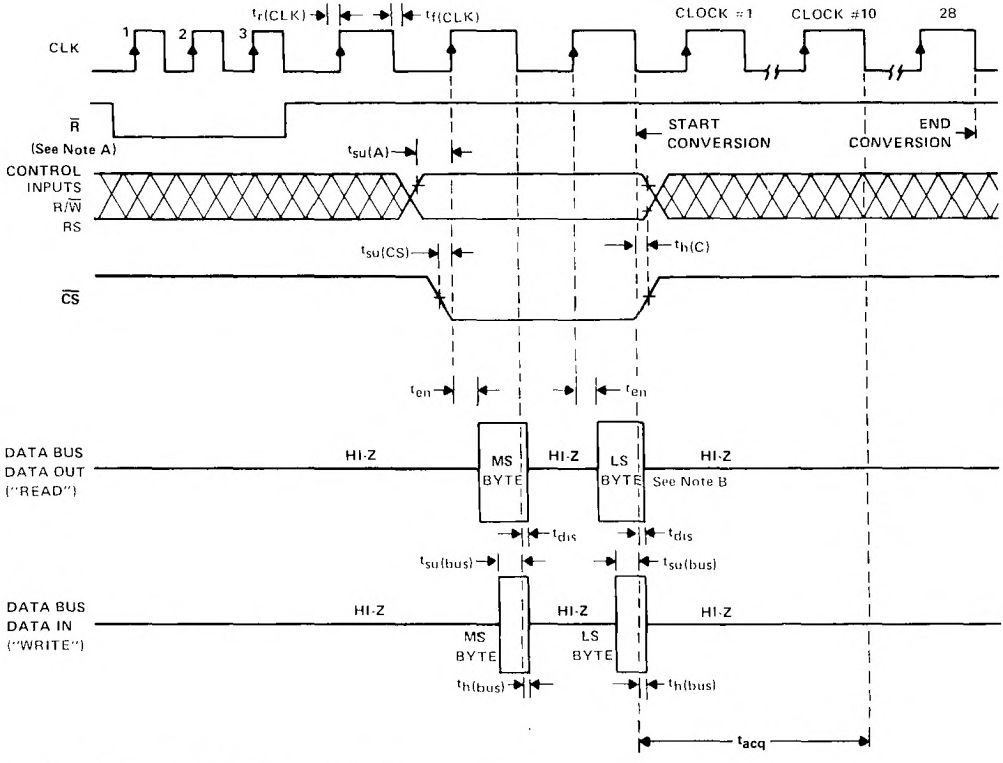


typical operating sequence



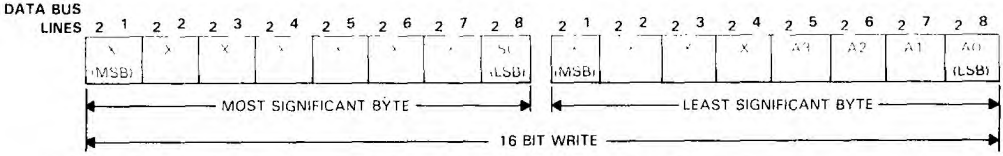
NOTES
A This is a 16-bit input instruction from the microprocessor being sent to the control data register
B This is the 2-byte (16-bit) content of the digital data register being sent to the microprocessor
C This is the LS byte (8-bit) content of the analog conversion data register being sent to the microprocessor
D This is the LS byte (8-bit) content of the digital data register being sent to the microprocessor
E These are MS byte (8-bit), LS byte (8-bit), and LS byte (8-bit) content of the analog conversion data register or digital data register being sent to the microprocessor
F This is the 2-byte (16-bit) content of the analog conversion data register being sent to the microprocessor

read or write cycle time sequence



NOTES: A. The reset pulse ($\overline{R}$ low) is required only during power-up.

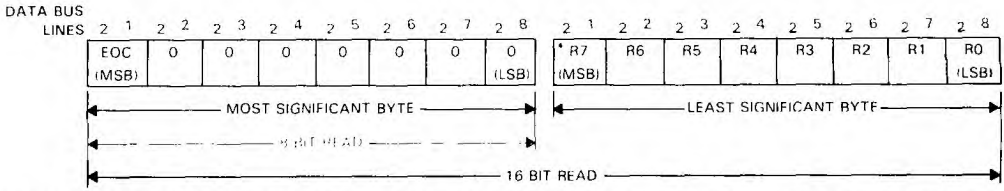
B. The most significant byte output of Data Out occurs when CLK is high. When CLK is low, Data Out is in the high-impedance (off) state. When CLK goes high again, the least significant byte is placed on the data bus. At this point, the least significant byte remains on the bus for as long as CLK is kept high.



Unused Bits (X) – The MS byte bits 2^{-1} through 2^{-7} and LS byte bits 2^{-1} through 2^{-4} of the control register are not used internally.
Start Conversion (SC) – When the SC bit in the MS byte is set to a logical 1, and analog-to-digital conversion on the specified analog channel begins immediately after the completion of the control register write
Analog Multiplex Address (A0-A3) – These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below:

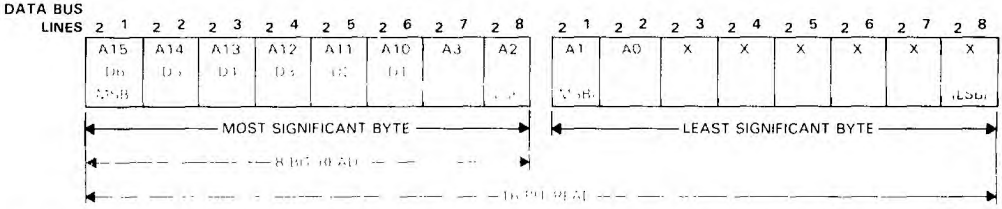
Hexadecimal Address (A3 – MSB)	Channel Select
0	A0
1	REF + (A1)
2-5	A2-A5
6 9 (not used)	
A-F	A10 A15

FIGURE 1. WORD FORMAT AND CONTENT FOR CONTROL REGISTER 2-BYTE WRITE



A/D Status (EOC) – The A/D status end-of-conversion (EOC) bit is set whenever an analog-to-digital conversion is successfully completed by the A/D converter. The status bit is cleared by a 16-bit write from the microprocessor to the control register. The remainder of the bits in the MS byte of the analog conversion data register are always reset to logical 0 to simplify microprocessor interrogation of the A/D converter status.
A/D Result (R0-R7) – The LS byte of the analog conversion data register contains the result of the analog-to-digital conversion. Result bit R7 is the MSB and the converter follows the standard convention of assigning a code of all ones (11111111) to a full-scale analog voltage. There are no special overflow or underflow indications.

FIGURE 2. WORD FORMAT AND CONTENT FOR ANALOG CONVERSION DATA REGISTER 1-BYTE AND 2-BYTE READ



Shared Digital Port (A10/D1-A15/D6) – The voltage present on these pins is interpreted as a digital signal, and the corresponding states are read from these bits. A digital value is given for each pin even if some or all of these pins are being used as analog inputs.
Analog Multiplexer Address (A0-A3) – The address of the selected analog channel presently addressed is given by these bits.
Unused Bits (X) – LS byte bits 2^{-3} through 2^{-8} of the digital data register are not used.

FIGURE 3. WORD FORMAT AND CONTENT FOR DIGITAL DATA REGISTER 1-BYTE AND 2-BYTE READ

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 6.5 V
Input voltage range: Positive reference voltage . . . . . V_{REF-} to V_{CC} + 0.3 V
Negative reference voltage . . . . . −0.3 V to V_{REF+}
All other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Input current, I_I (any input) . . . . . ±10 mA
Total input current, (all inputs) . . . . . ±20 mA
Operating free-air temperature range: TLC532AM, TLC533AM . . . . . −55°C to 125°C
TLC532AI, TLC533AI . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Case temperature for 10 seconds: FN package . . . . . 260°C

NOTE 1 All voltage values are with respect to network ground terminal.

recommended operating conditions

		TLC532A			TLC533A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)		2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)		−0.1	0	2.5	−0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$		1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
High-level input voltage, V_{IH}	Clock input	$V_{CC}-0.8$			$V_{CC}-0.8$			V
	All other digital inputs	2			2			
Low-level input voltage, V_{IL}	Any digital input			0.8			0.8	V
Clock frequency, f_{CLK}		0.1	2	2.048	0.1	1.048	1.06	MHz
CS setup time, $t_{su(CS)}$		75			100			ns
Address (R/W and RS) setup time, $t_{su(A)}$		100			145			ns
Data bus input setup time, $t_{su(bus)}$		140			185			ns
Control (R/W, RS, and CS) hold time, $t_{h(C)}$		10			20			ns
Data bus input hold time, $t_{h(bus)}$		15			20			ns
Pulse duration of control during read, $t_{w(C)}$		305			575			ns
Pulse duration, reset low, $t_{wL(reset)}$		3			3			Clock Cycles
Pulse duration of clock high, $t_{wH(CLK)}$		230			440			ns
Pulse duration of clock low, $t_{wL(CLK)}$		200			410			ns
Clock rise time, $t_{r(CLK)}$				15			25	ns
Clock fall time, $t_{f(CLK)}$				16			30	ns
Operating free-air temperature, T_A	TLC_ _AM	−55		125	−55		125	°C
	TLC_ _AI	−40		85	−40		85	

NOTE 2: Analog input voltages greater than or equal to that applied to the REF+ terminal convert to all ones (11111111), while input voltages equal to or less than that applied to the REF− terminal convert to all zeros (00000000). For proper operation, the positive reference voltage, V_{REF+}, must be at least 1 V greater than the negative reference voltage, V_{REF-}. In addition, unadjusted errors may increase as the differential reference voltage, $V_{REF+} - V_{REF-}$, falls below 4.75 V.

electrical characteristics over recommended operating free-air temperature range, $V_{REF+} = V_{CC}$, V_{REF-} at ground, $f_{CLK} = 2$ MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = -1.6$ mA	2.4			V
V_{OL}	Low-level output voltage		$I_{OL} = 1.6$ mA			0.4	V
I_{IH}	High-level input current	Any digital or Clock input	$V_{IH} = 5.5$ V			10	μA
		Any control input				1	
I_{IL}	Low-level input current	Any digital or Clock input	$V_{IL} = 0$			−10	μA
		Any control input				−1	
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{CC}$			10	μA
			$V_O = 0$			−10	
I_I	Analog input current (see Note 3)		$V_I = 0$ to V_{CC}			±500	nA
	Leakage current between selected channel and all other analog channels		$V_I = 0$ to V_{CC}, Clock input at 0 V			±400	nA
C_i	Input capacitance	Digital pins 3 thru 10			4	30	pF
		Any other input pin			2	15	
$I_{CC}+I_{REF+}$	Supply current plus reference current		$V_{CC} = V_{REF+} = 5.5$ V, Outputs open		1.5	3	mA
I_{CC}	Supply current		$V_{CC} = 5.5$ V		1.4	2	mA

NOTE 3: Analog input current is an average of the current flowing into a selected analog channel input during one full conversion cycle.

operating characteristics over recommended operating free-air temperature range, $V_{REF+} = V_{CC}$, V_{REF-} at ground, $f_{CLK} = 2$ MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error (see Note 4)					±0.5	LSB
	Zero error (see Note 5)					±0.5	LSB
	Full-scale error (see Note 5)					±0.5	LSB
	Total unadjusted error (see Note 6)					±0.5	LSB
	Absolute accuracy error (see Note 7)					±1	LSB
t_{conv}	Conversion time (including channel acquisition time)				30		Clock Cycles
t_{acq}	Channel acquisition time prior to starting conversion				10		Clock Cycles
t_{en}	Data output enable time (see Note 8)		$C_L = 50$ pF, $R_L = 3$ kΩ,			250	ns
t_{dis}	Data output disable time		$C_L = 50$ pF, $R_L = 3$ kΩ	10			ns
$t_{r(bus)}$	Data bus output rise time	High impedance to high level	$C_L = 50$ pF, $R_L = 3$ kΩ				ns
		Low-to-high level					
$t_{f(bus)}$	Data bus output fall time	High impedance to low level	$C_L = 50$ pF, $R_L = 3$ kΩ				ns
		High-to-low level				300	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTES: 4. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
5. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
6. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
7. Absolute accuracy error is the maximum difference between an analog value and the nominal midstep value within any step. This includes all errors including inherent quantization error, which is the ±0.5 LSB uncertainty caused by the A/D converters' finite resolution.
8. If chip-select setup time, $t_{su(CS)}$, is less than 0.14 μs, the effective data output enable time, t_{en}, may extend such that $t_{su(CS)} + t_{en}$ is equal to a maximum of 0.475 μs.

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electrical characteristics over recommended ranges V_{CC}, V_{REF+}, and operating free-air temperature, V_{REF-} at ground, f_{CLK} = 1.048 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1.6 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current	Any digital or Clock input	V_{IH} = 5.5 V			10	μA
		Any control input				1	
I_{IL}	Low-level input current	Any digital or Clock input	V_{IL} = 0			−10	μA
		Any control input				−1	
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{CC}$			10	μA
			V_O = 0			−10	
I_I	Analog input current (see Note 3)		V_I = 0 to V_{CC}			±500	nA
	Leakage current between selected channel and all other analog channels		V_I = 0 to V_{CC}, Clock input at 0 V			±400	nA
C_i	Input capacitance	Digital pins 3 thru 10			4	30	pF
		Any other input pin			2	15	
$I_{CC}+I_{REF+}$	Supply current plus reference current		$V_{CC} = V_{REF+}$ = 5.5 V, Outputs open		1.3	3	mA
I_{CC}	Supply current		V_{CC} = 5.5 V		1.2	2	mA

NOTE 3: Analog input current is an average of the current flowing into a selected analog channel input during one full conversion cycle.

operating characteristics over recommended ranges V_{CC}, V_{REF+}, and operating free-air temperature, V_{REF-} at ground, f_{clock} = 1.048 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error (see Note 4)					±0.5	LSB
	Zero error (see Note 5)					±0.5	LSB
	Full-scale error (see Note 5)					±0.5	LSB
	Total unadjusted error (see Note 6)					±0.5	LSB
	Absolute accuracy error (see Note 7)					±1	LSB
t_{conv}	Conversion time (including channel acquisition time)				30		Clock Cycles
t_{acq}	Channel acquisition time prior to starting conversion				10		Clock Cycles
t_{en}	Data output enable time (see Note 8)		C_L = 50 pF, R_L = 3 kΩ,			335	ns
t_{dis}	Data output disable time		C_L = 50 pF, R_L = 3 kΩ	10			ns
$t_{r(bus)}$	Data bus output rise time	High impedance to high level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		Low-to-high level				300	
$t_{f(bus)}$	Data bus output fall time	High impedance to low level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		High-to-low level				300	

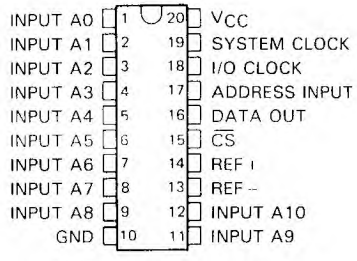
† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
5. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
6. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
7. Absolute accuracy error is the maximum difference between an analog value and the nominal midstep value within any step. This includes all errors including inherent quantization error, which is the ±0.5 LSB uncertainty caused by the A/D converters' finite resolution.
8. If chip-select setup time, $t_{su(CS)}$, is less than 0.14 μs, the effective data output enable time, t_{en}, may extend such that $t_{su(CS)} + t_{en}$ is equal to a maximum of 0.475 μs.

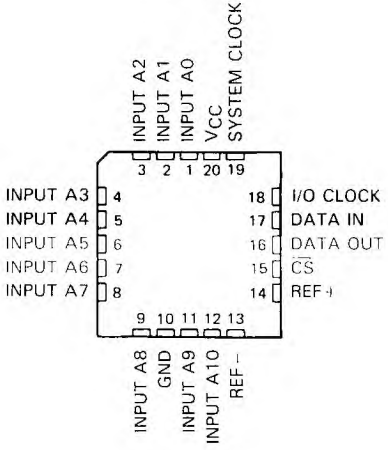
D2799, OCTOBER 1983 - REVISED OCTOBER 1988

- LinCMOS™ Technology
- 8-Bit Resolution A/D Converter
- Microprocessor Peripheral or Stand-Alone Operation
- On-Chip 12-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- TLC541 is Direct Replacement for Motorola MC145040 and National Semiconductor ADC0811. TLC540 is Capable of Higher Speed
- Pinout and Control Signals Compatible with TLC1540 Family of 10-Bit A/D Converters

DW OR N PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



TYPICAL PERFORMANCE	TLC540	TLC541
Channel Acquisition Sample Time	2 μs	3.6 μs
Conversion Time	9 μs	17 μs
Samples per Second	75 × 10^3	40 × 10^3
Power Dissipation	6 mW	6 mW

description

The TLC540 and TLC541 are LinCMOS™ A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a three-state output with up to four control inputs [including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input]. A 4-MHz system clock for the TLC540 and a 2.1-MHz system clock for the TLC541 with a design that includes simultaneous read/write operation allow high-speed data transfers and sample rates of up to 75,180 samples per second for the TLC540 and 40,000 samples per second for the TLC541. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The converters incorporated in the TLC540 and TLC541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A switched-capacitor design allows low-error (±0.5 LSB) conversion in 9 μs for the TLC540 and 17 μs for the TLC541 over the full operating temperature range.

The M-suffix versions are characterized for operation from −55°C to 125°C. The I-suffix versions are characterized for operation from −40°C to 85°C.

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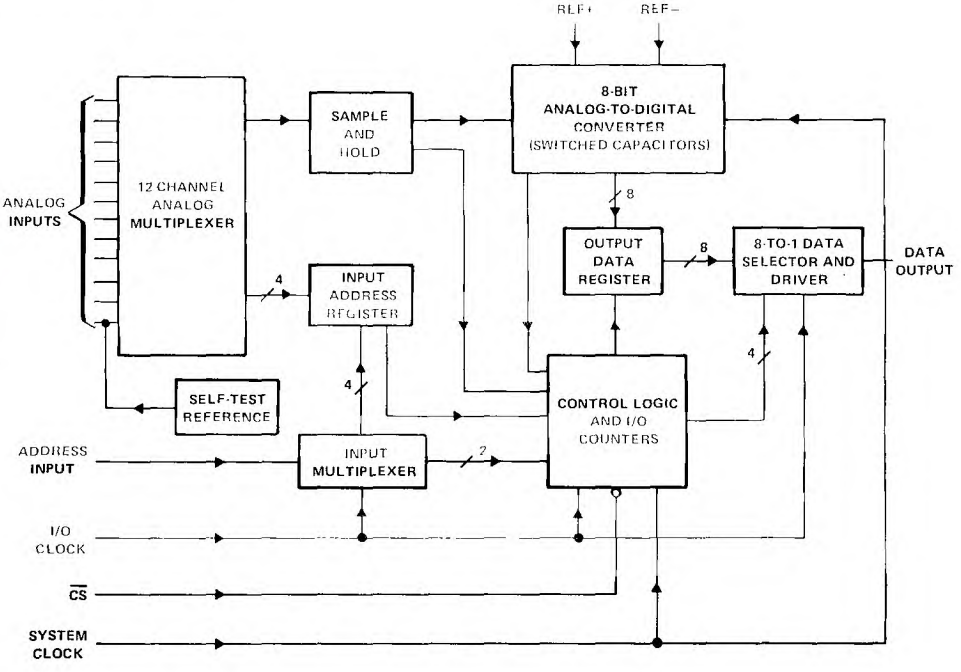
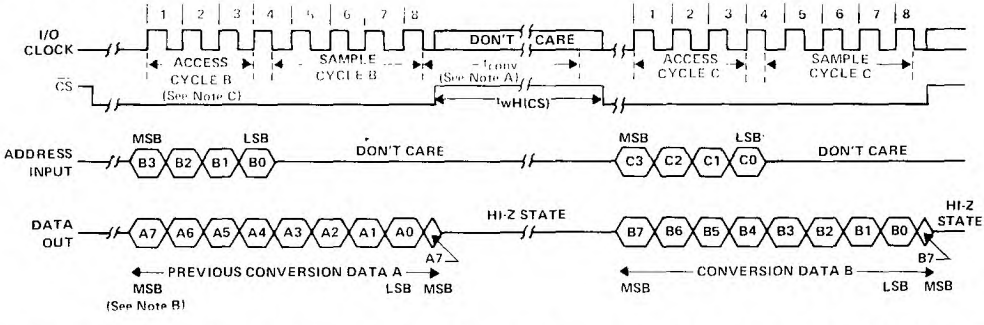
functional block diagram



operating sequence



NOTES A. The conversion cycle, which requires 36 System Clock periods, is initiated on the 8th falling edge of the I/O Clock after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, the I/O Clock must remain low for at least 36 System Clock cycles to allow conversion to be completed.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O Clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three System Clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range (any input) . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range: TLC540I, TLC541I . . . . . −40°C to 85°C
TLC540M, TLC541M . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to digital ground with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

			TLC540			TLC541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)			−0.1	0	2.5	0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLK↑, $t_{su(A)}$			200			400			ns
Hold time, address bits after I/O CLK↑, $t_{h(A)}$			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			3			System clock cycles
$\overline{CS}$ high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0		2.048	0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		4	$f_{CLK(I/O)}$		2.1	MHz
System clock high, $t_{wH(SYS)}$			110			210			ns
System clock low, $t_{wL(SYS)}$			100			190			ns
Input/Output clock high, $t_{wH(I/O)}$			200			404			ns
Input/Output clock low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \le 1048$ kHz			30			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC540M, TLC541M	−55		125	−55		125	°C
		TLC540I, TLC541I	−40		85	−40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

3. To minimize errors caused by noise at the chip select input, the internal circuitry waits for three System Clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor

electrical characteristics over recommended operating temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC540 or $f_{CLK(I/O)}$ = 1.1 MHz for TLC541

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 16)		V_{CC} = 4.75 V,	I_{OH} = 360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 1.6 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
I_{CC} + I_{REF}	Supply and reference current		V_{REF+} = V_{CC},	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

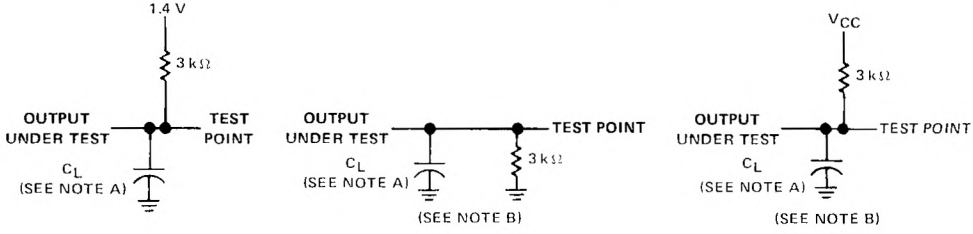
†All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V, $f_{CLK(I/O)}$ = 2.048 MHz for TLC540 or 1.1 MHz for TLC541, $f_{CLK(SYS)}$ = 4 MHz for TLC540 or 2.1 MHz for TLC541.

PARAMETER		TEST CONDITIONS	TLC540			TLC541			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Linearity error	See Note 5			±0.5			±0.5	LSB
	Zero error	See Notes 2 and 6			±0.5			±0.5	LSB
	Full-scale error	See Notes 2 and 6			±0.5			±0.5	LSB
	Total unadjusted error	See Note 7			±0.5			±0.5	LSB
	Self-test output code	Input A11 address = 1011 (See Note 8)	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence			9			17	μs
	Total access and conversion time	See Operating Sequence			13.3			25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			4			4	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time, I/O clock↓ to data output valid	See Parameter Measurement Information			300			400	ns
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150				ns
$t_{r(bus)}$	Data bus rise time				300				ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all "1"s (11111111), while input voltages less than that applied to REF− convert to all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics
6. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic.

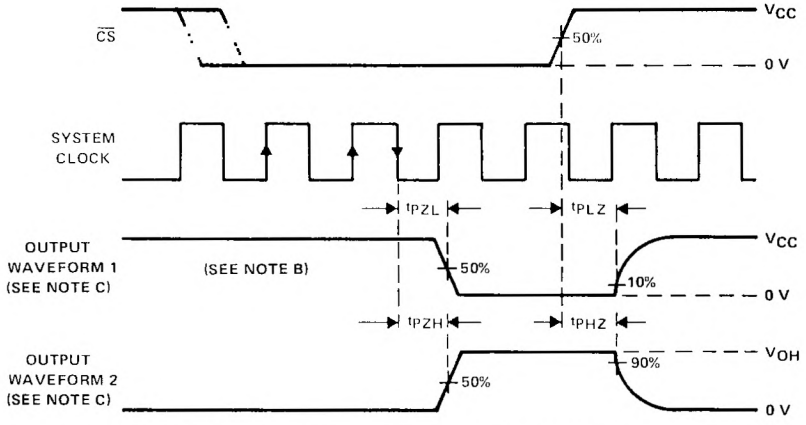
PARAMETER MEASUREMENT INFORMATION



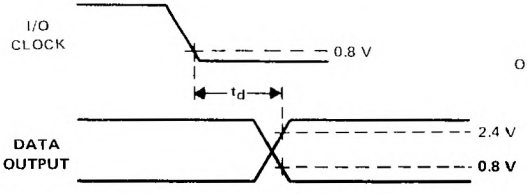
LOAD CIRCUIT FOR t_d, t_r, AND t_f

LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME

VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC540 and 100 pF for TLC541.
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC540 and TLC541 are each complete data acquisition systems on a single chip. They include such functions as analog multiplexer, sample-and-hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs [two clocks, chip select ($\overline{CS}$), and address]. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, with TLC540 a conversion can be completed in 9 μs, while complete input-conversion-output cycles can be repeated every 13 μs. With TLC541 a conversion can be completed in 17 μs, while complete input-conversion-output cycles are repeated every 25 μs. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in "self-test," and in any order desired by the controlling processor.

The System and I/O Clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the System Clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O Clock. The System Clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the Data Output pin is in a three-state condition and the Address Input and I/O Clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$ pin, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC540/541 devices are used. In this way, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the System Clock after a low $\overline{CS}$ transition, before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result will automatically appear on the Data Out pin.
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of the I/O Clock. The MSB of the address is shifted in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three clock cycles are then applied to the I/O pin and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to the I/O Clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 System Clock cycles. After this final I/O Clock cycle, $\overline{CS}$ must go high or the I/O Clock must remain low for at least 36 System Clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 System Clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the System and I/O Clock pins together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O Clock. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the ''conversion crunching'' circuitry.
2. The device will recognize a $\overline{CS}$ low transition only when the $\overline{CS}$ input changes and subsequently the System Clock pin receives two positive edges and then a negative edge. For this reason, after a negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O Clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the sixth I/O Clock pulse that has been recognized by the device, so that a $\overline{CS}$ low level will be recognized upon the lowering of the eighth I/O Clock signal that is recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O Clock pulses and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the fourth I/O Clock cycle, the hold function is not initiated until the negative edge of the eighth I/O Clock cycle. Thus, the control circuitry can leave the I/O Clock signal in its high state during the eighth I/O Clock cycle until the moment at which the analog signal must be converted. The TLC540/TLC541 will continue sampling the analog input until the eighth falling edge of the I/O Clock. The control circuitry or software will then immediately lower the I/O Clock signal and hold the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

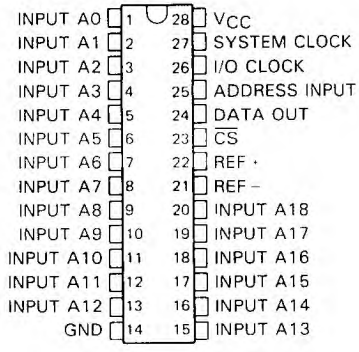
TLC545M, TLC545I, TLC545C, TLC546M, TLC546I, TLC546C
LinCMOS™ 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH SERIAL CONTROL AND 19 INPUTS

D2850, DECEMBER 1985—REVISED SEPTEMBER 1988

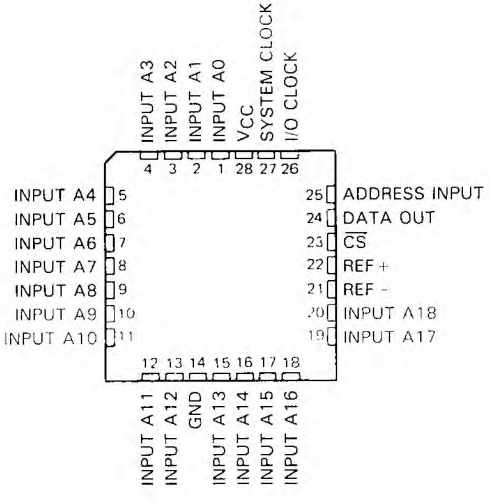
- LinCMOS™ Technology
- 8-Bit Resolution A/D Converter
- Microprocessor Peripheral or Stand-Alone Operation
- On-Chip 20-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- Timing and Control Signals Compatible with 8-Bit TLC540 and 10-Bit TLC1540 A/D Converter Families

TYPICAL PERFORMANCE	TL545	TL546
Channel Acquisition Time	1.5 μs	2.7 μs
Conversion Time	9 μs	17 μs
Sampling Rate	76 × 10^3	40 × 10^3
Power Dissipation	6 mW	6 mW

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The TLC545 and TLC546 are LinCMOS™ A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs [including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input]. A 4-MHz system clock for the TLC545 and a 2.1-MHz system clock for the TLC546 with a design that includes simultaneous read/write operation allowing high-speed data transfers and sample rates of up to 76,923 samples per second for the TLC545, and 40,000 samples per second for the TLC546. In addition to the high-speed converter and versatile control logic, there is an on-chip 20-channel analog multiplexer that can be used to sample any one of 19 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under microprocessor control.

The converters incorporated in the TLC545 and TLC546 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows low-error (±0.5 LSB)

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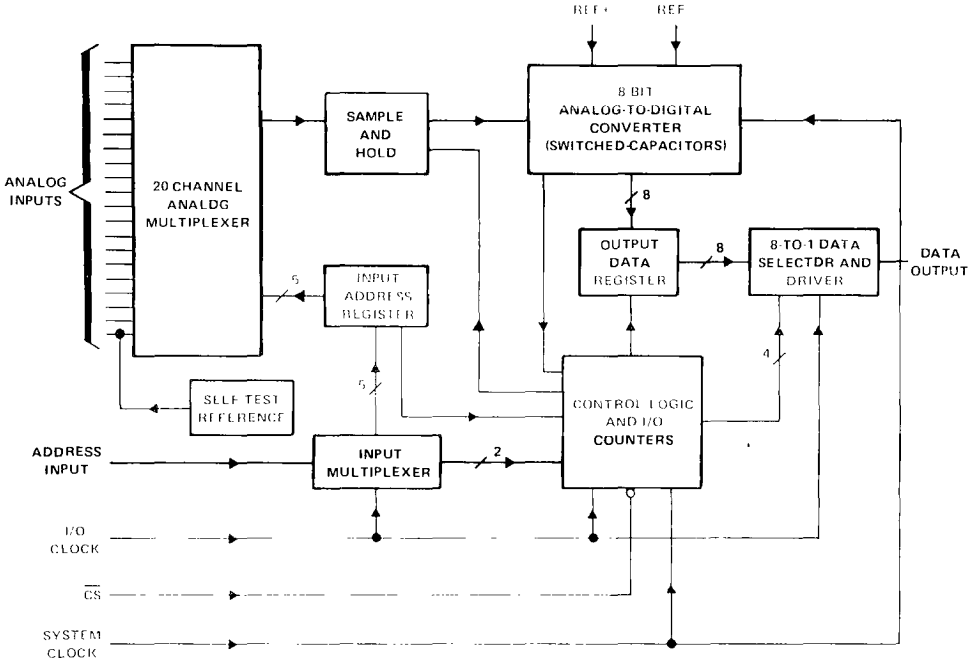
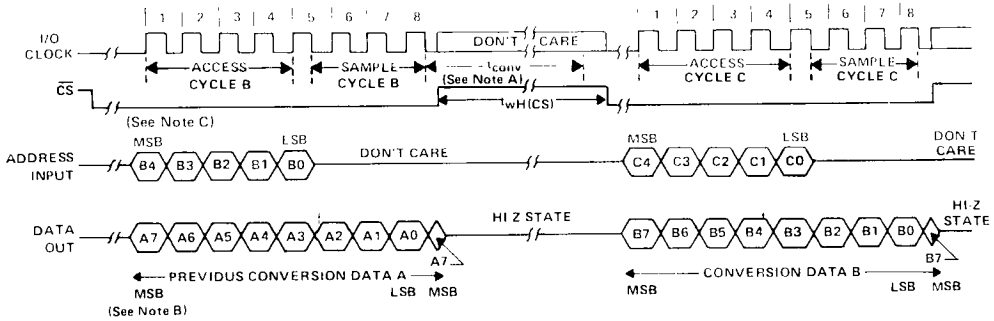
conversion in 9 μs for the TLC545, and 17 μs for the TLC546, over the full operating temperature range. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The TLC545M and the TLC546M are characterized for operation from −55°C to 125°C. The TLC545I and the TLC546I are characterized for operation from −40°C to 85°C. The TLC545C and the TLC546C are characterized for operation from 0°C to 70°C.

functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 36 system clock periods, is initiated with the 8th I/O clock↓ after CS↓ for the channel whose address exists in memory at that time.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three system clock cycles (or less) after a chip select transition before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range (any input) . . . . . −0.3 V to V_{CC} +0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} +0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range: TLC545M, TLC546M . . . . . −55°C to 125°C
TLC545I, TLC546I . . . . . −40°C to 85°C
TLC545C, TLC546C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

			TLC545			TLC546			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 3)			0	V_{CC}	$V_{CC}+0.1$	0	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{ref-} (see Note 2)			−0.1	0	V_{CC}	−0.1	0	V_{CC}	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)			0	V_{CC}	$V_{CC}+0.2$	0	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLK↑, $t_{su(A)}$			200			200			ns
Address hold time, t_h			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			3			System clock cycles
Chip select high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0		2.048	0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		4	$f_{CLK(I/O)}$		2.1	MHz
System clock high, $t_{wH(SYS)}$			110			210			ns
System clock low, $t_{wL(SYS)}$			110			190			ns
Input/Output clock high, $t_{wH(I/O)}$			200			404			ns
Input/Output clock low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \le 1048$ kHz			30			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{CLK(I/O)} \le 1.024$ MHz			100			100	ns
		$f_{CLK(I/O)} > 1.024$ MHz			40			40	
Operating free-air temperature, T_A		TLC545M, TLC546M	−55		125	−55		125	°C
		TLC545I, TLC546I	−40		85	−40		85	
		TLC545C, TLC546C	0		70	0		70	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). As the differential reference voltage decreases below 4.75 V, the total unadjusted error tends to increase.

3. To minimize errors caused by noise at the Chip Select input, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge or rising edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{ref+} = 4.75$ V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)} = 2.048$ MHz for TLC545 or $f_{CLK(I/O)} = 1.1$ MHz for TLC546

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 24)		V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		$V_I = V_{CC}$			0	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
$I_{CC} + I_{ref}$	Supply and reference current		$V_{ref+} = V_{CC}$,	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

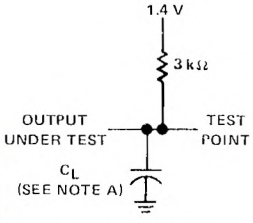
†All typical values are at T_A = 25°C

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 4.75$ V to 5.5 V, $f_{CLK(I/O)} = 2.048$ MHz for TLC545 or 1.1 MHz for TLC546, $f_{CLK(SYS)} = 4$ MHz for TLC545 or 2.1 MHz for TLC546

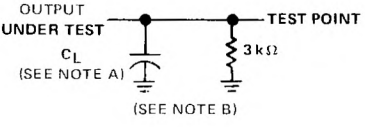
PARAMETER		TEST CONDITIONS	TLC545			TLC546			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Linearity error	See Note 5			±0.5			±0.5	LSB
	Zero error	See Note 6			±0.5			±0.5	LSB
	Full-scale error	See Note 6			±0.5			±0.5	LSB
	Total unadjusted error	See Note 7						±0.5	LSB
	Self-test output code	Input A19 address = 10011 (See Note 8)	01111101 (125)		100 1 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence			9			17	μs
	Total access and conversion time	See Operating Sequence			13			25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			3			3	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time, I/O clock↓ to data output valid	See Parameter Measurement Information			300			400	ns
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

NOTES: 5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero Error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A19 analog input signal is internally generated and is used for test purposes

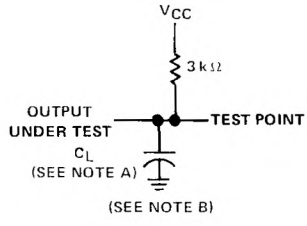
PARAMETER MEASUREMENT INFORMATION



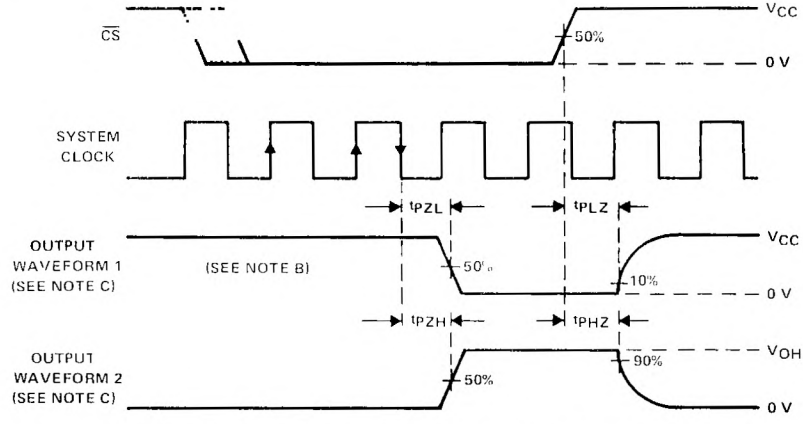
LOAD CIRCUIT FOR t_d, t_r, AND t_f



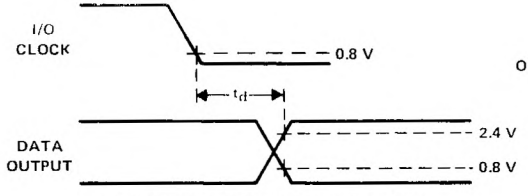
LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}



LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME

VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC545 and 100 pF for TLC546
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

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principles of operation

The TLC545 and TLC546 are both complete data acquisition systems on single chips. Each includes such functions as system clock, sample-and-hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs; Chip Select ($\overline{CS}$), Address Input, I/O clock, and System clock. These control inputs and a TTL-compatible 3-state output facilitate serial communications with a microprocessor or microcomputer. The TLC545 and TLC546 can complete conversions in a maximum of 9 and 17 μs respectively, while complete input-conversion-output cycles can be repeated at a maximum of 13 and 25 μs, respectively.

The System and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the System clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O clock. The System clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the Data Output pin is in a high-impedance condition, and the Address Input and I/O Clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC545/TLC546 devices are used. Thus, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the System clock after a $\overline{CS}$ transition before the transition is recognized. The MSB of the previous conversion result will automatically appear on the Data Out pin.
2. A new positive-logic multiplexer address is shifted in on the first five rising edges of the I/O clock. The MSB of the address is shifted in first. The negative edges of these five I/O clocks shift out the 2nd, 3rd, 4th, 5th, and 6th most significant bits of the previous conversion result. The on-chip sample-and hold begins sampling the newly addressed analog input after the 5th falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Two clock cycles are then applied to the I/O pin and the 7th and 8th conversion bits are shifted out on the negative edges of these clock cycles.
4. The final 8th clock cycle is applied to the I/O clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 system clock cycles. After this final I/O clock cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 36 system clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the system and I/O clocks together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

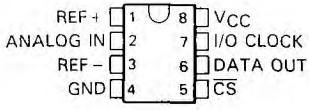
1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O clock. When the $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the "conversion crunching" circuitry.
2. The device will recognize a $\overline{CS}$ transition only when the $\overline{CS}$ input changes and subsequently the system clock pin receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the 6th I/O clock, which has been recognized by the device, so that a $\overline{CS}$ low level will be recognized upon the lowering of the 8th I/O clock signal recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O clocks and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the 5th I/O clock cycle, the hold function is not initiated until the negative edge of the 8th I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the 8th I/O clock cycle, until the moment at which the analog signal must be converted. The TLC545/546 will continue sampling the analog input until the 8th falling edge of the I/O clock. The control circuitry or software must then immediately lower the I/O clock signal to initiate the hold function at the desired point in time and to start conversion.

Detailed information on interfacing to most popular microprocesors is readily available from the factory.

- LinCMOS™ Technology
- Microprocessor Peripheral or Stand-Alone Operation
- 8-Bit Resolution A/D Converter
- Differential Reference Input Voltages
- Conversion Time . . . 17 μs Max
- Total Access and Conversion Cycles Per Second
  TLC548 . . . up to 45,500
  TLC549 . . . up to 40,000
- On-Chip Software-Controllable Sample-and-Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- 4-MHz Typical Internal System Clock
- Wide Supply Range . . . 3 V to 6 V
- Low Power Consumption . . . 6 mW Typ
- Ideal for Cost-Effective, High-Performance Applications Including Battery-Operated Portable Instrumentation
- Pinout and Control Signals Compatible with the TLC540 and TLC545 8-Bit A/D Converters and with the TLC1540 10-Bit A/D Converter

D OR P PACKAGE
(TOP VIEW)



description

The TLC548 and TLC549 are LinCMOS™ A/D peripheral integrated circuits built around an 8-bit switched-capacitor successive-approximation ADC. They are designed for serial interface with a microprocessor or peripheral through a 3-state data output and an analog input. The TLC548 and TLC549 use only the Input/Output Clock (I/O Clock) input along with the Chip Select ($\overline{CS}$) input for data control. The maximum I/O clock input frequency of the TLC548 is guaranteed up to 2.048 MHz, and the I/O clock input frequency of the TLC549 is guaranteed to 1.1 MHz. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

Operation of the TLC548 and the TLC549 is very similar to that of the more complex TLC540 and TLC541 devices; however, the TLC548 and TLC549 provide an on-chip system clock that operates typically at 4 MHz and requires no external components. The on-chip system clock allows internal device operation to proceed independently of serial input/output data timing and permits manipulation of the TLC548 and TLC549 as desired for a wide range of software and hardware requirements. The I/O Clock together with the internal system clock allow high-speed data transfer and conversion rates of 45,500 conversions per second for the TLC548, and 40,000 conversions per second for the TLC549.

Additional TLC548 and TLC549 features include versatile control logic, an on-chip sample-and-hold circuit that can operate automatically or under microprocessor control, and a high-speed converter with differential high-impedance reference voltage inputs that ease ratiometric conversion, scaling, and circuit isolation from logic and supply noises. Design of the totally switched-capacitor successive-approximation converter circuit allows conversion with a maximum total error of ±0.5 least significant bit (LSB) in less than 17 μs.

The TLC548M and TLC549M are characterized for operation over the temperature range of −55°C to 125°C. The TLC548I and TLC549I are characterized for operation from −40°C to 85°C. The TLC548C and TLC549C are characterized for operation from 0°C to 70°C.

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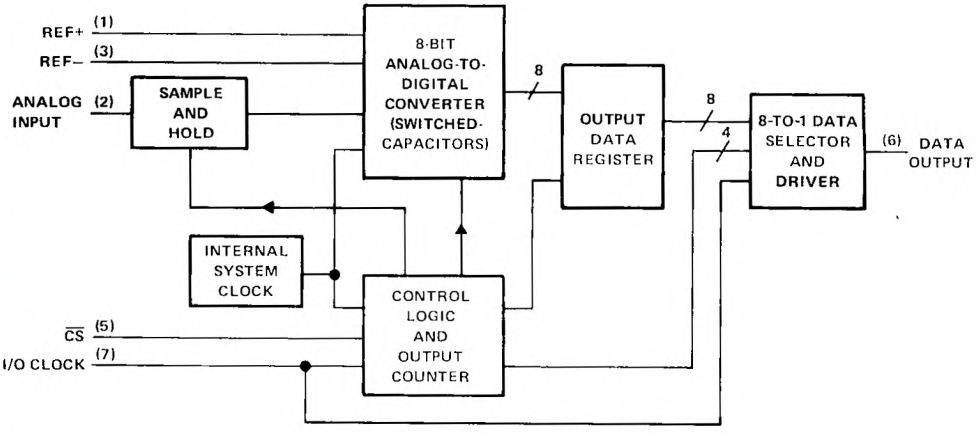
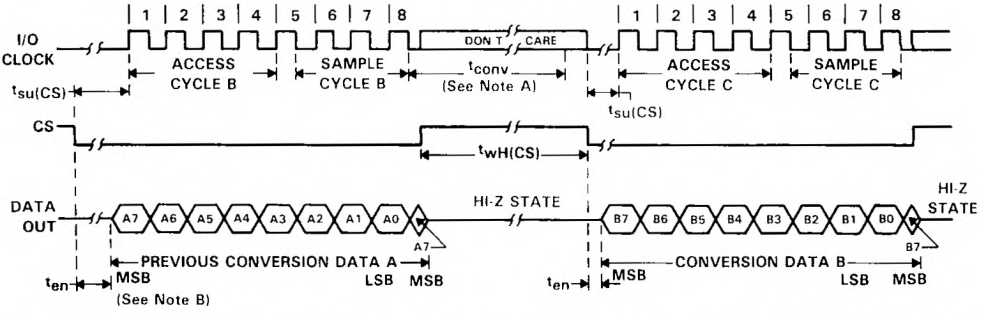
functional block diagram



operating sequence



NOTES. A. The conversion cycle, which requires 36 internal system clock periods (17 μs maximum), is initiated with the 8th I/O clock pulse trailing edge after $\overline{CS}$ goes low for the channel whose address exists in memory at the time.

B. The most significant bit (A7) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O clock falling edges. B7-B0 will follow in the same manner.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range at any input . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current range (all inputs) . . . . . ±30 mA
Operating free-air temperature range (see Note 2): TLC548M, TLC549M . . . . . −55°C to 125°C
TLC548I, TLC549I . . . . . −40°C to 85°C
TLC548C, TLC549C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1 All voltage values are with respect to the network ground terminal with the REF− and GND terminal pins connected together, unless otherwise noted.
2. The D package is not recommended below −40°C.

recommended operating conditions

		TLC548			TLC549			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		3	5	6	3	5	6	V
Positive reference voltage, V_{REF+} (see Note 3)		2.5	V_{CC}	V_{CC}+0.1	2.5	V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{REF-} (see Note 3)		−0.1	0	2.5	−0.1	0	2.5	V
Differential reference voltage, V_{REF+}, V_{REF-} (see Note 3)		1	V_{CC}	V_{CC}+0.2	1	V_{CC}	V_{CC}+0.2	V
Analog input voltage (see Note 3)		0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH} (for V_{CC} = 4.75 V to 5.5 V)		2			2			V
Low-level control input voltage, V_{IL} (for V_{CC} = 4.75 V to 5.5 V)				0.8			0.8	V
Input/output clock frequency, $f_{CLK(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		0		2.048	0		1.1	MHz
Input/output clock high, $t_{wH(I/O)}$ (for V_{CC} = 4.75 V to 5.5 V)		200			404			ns
Input/output clock low, t_{wl} for V_{CC} = 4.75 V to 5.5 V)		200			404			ns
Input/output clock transition time, $t_{t(I/O)}$ (see Note 4) (for V_{CC} = 4.75 V to 5.5 V)				100			100	ns
Duration of $\overline{CS}$ input high state during conversion, $t_{wH(CS)}$ (for V_{CC} = 4.75 V to 5.5 V)		17			17			μs
Setup time, $\overline{CS}$ low before first I/O clock, $t_{su(CS)}$ (for V_{CC} = 4.75 V to 5.5 V) (see Note 5)		1.4			1.4			μs
Operating free-air temperature, T_A	TLC548M, TLC549M	−55		125	−55		125	°C
	TLC548I, TLC549I	−40		85	−40		85	
	TLC548C, TLC549C	0		70	0		70	

NOTES: 3. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF− convert to all zeros (00000000). For proper operation, the positive reference voltage V_{REF+}, must be at least 1 V greater than the negative reference voltage V_{REF-}. In addition, unadjusted errors may increase as the differential reference voltage $V_{REF+} - V_{REF-}$ falls below 4.75 V.
4 This is the time required for the input/output clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications in which the sensor and the ADC are placed several feet away from the controlling microprocessor.
5. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and one falling edge of internal system clock after $\overline{CS}$↓ before responding to control input signals. This $\overline{CS}$ set-up time is given by the t_{en} and $t_{su(CS)}$ specifications.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC548 or 1.1 MHz for TLC549

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.75 V, I_{OH} = −360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC}, $\overline{CS}$ at V_{CC}			10	V
			V_O = 0, $\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current, control inputs		V_I = V_{CC}		0.005	2.5	μA
I_{IL}	Low-level input current, control inputs		V_I = 0		−0.005	−2.5	μA
$I_{I(on)}$	Analog channel on-state input current, during sample cycle		Analog input at V_{CC}		0.4	1	μA
			Analog input at 0 V		−0.4	−1	
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V		1.8	2.5	mA
I_{CC} + I_{REF}	Supply and reference current		V_{REF+} = V_{CC}		1.9	3	mA
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	

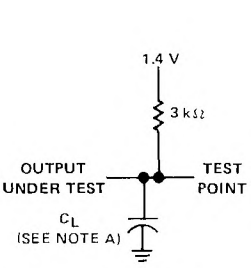
operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 2.048 MHz for TLC548 or 1.1 MHz for TLC549

PARAMETER		TEST CONDITIONS	TLC548			TLC549			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
	Linearity error	See Note 6			±0.5			±0.5	LSB
	Zero error	See Note 7			±0.5			±0.5	LSB
	Full-scale error	See Note 7			±0.5			±0.5	LSB
	Total unadjusted error	See Note 8			±0.5			±0.5	LSB
t_{conv}	Conversion time	See Operating Sequence		8	17		12	17	μs
	Total access and conversion time	See Operating Sequence		12	22		19	25	μs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			4			4	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time to data output valid	I/O clock↓			300			400	ns
t_{en}	Output enable time				1.4			1.4	μs
t_{dis}	Output disable time	See Parameter Measurement Information			150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

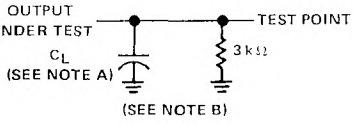
†All typicals are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 6. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
8. Total unadjusted error is the sum of linearity, zero, and full-scale errors.

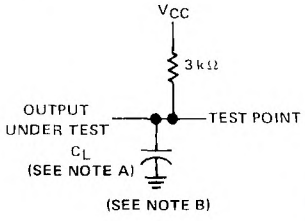
PARAMETER MEASUREMENT INFORMATION



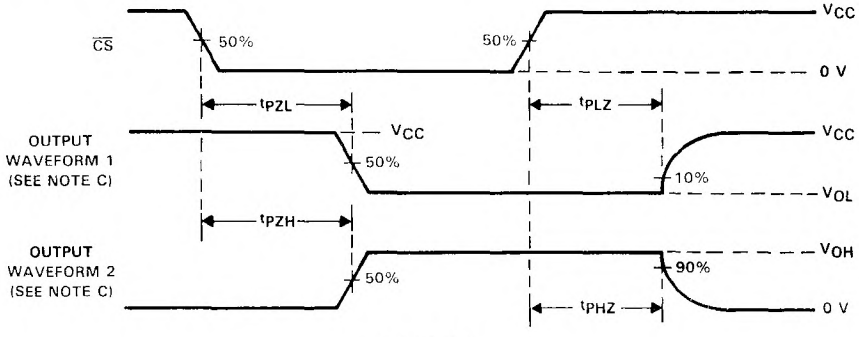
LOAD CIRCUIT FOR t_d, t_r, AND t_f



LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

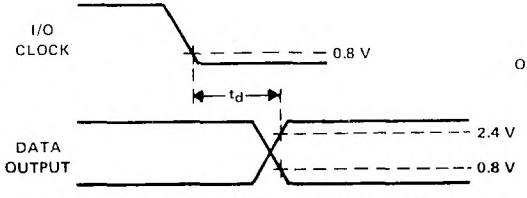


LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



(SEE NOTE B)

VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME

VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC548 and 100 pF for TLC549; C_L includes jig capacitance.
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

PRINCIPLES OF OPERATION

The TLC548 and TLC549 are each complete data acquisition systems on a single chip. Each contains an internal system clock, sample-and-hold, 8-bit A/D converter, data register, and control logic circuitry. For flexibility and access speed, there are two control inputs: I/O Clock and Chip Select ($\overline{CS}$). These control inputs and a TTL-compatible three-state output facilitate serial communications with a microprocessor or minicomputer. A conversion can be completed in 17 μs or less, while complete input-conversion-output cycles can be repeated in 22 μs for the TLC548 and in 25 μs for the TLC549.

The internal system clock and I/O clock are used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Due to this independence and the internal generation of the system clock, the control hardware and software need only be concerned with reading the previous conversion result and starting the conversion by using the I/O clock. In this manner, the internal system clock drives the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the data output pin is in a high-impedance condition and the I/O clock pin is disabled. This $\overline{CS}$ control function allows the I/O Clock pin to share the same control logic point with its counterpart pin when additional TLC548 and TLC549 devices are used. This also serves to minimize the required control logic pins when using multiple TLC548 and TLC549 devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the internal system clock after a $\overline{CS}\downarrow$ before the transition is recognized. However, upon a $\overline{CS}$ rising edge, DATA OUT will go to a high-impedance state within the t_{dis} specification even though the rest of the IC's circuitry will not recognize the transition until the $t_{su(CS)}$ specification has elapsed. This technique is used to protect the device against noise when used in a noisy environment. The most significant bit (MSB) of the previous conversion result will initially appear on the DATA OUT pin when $\overline{CS}$ goes low.
2. The falling edges of the first four I/O clock cycles shift out the 2nd, 3rd, 4th, and 5th most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the analog input after the 4th high-to-low transition of the I/O Clock. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three more I/O clock cycles are then applied to the I/O pin and the 6th, 7th, and 8th conversion bits are shifted out on the falling edges of these clock cycles.
4. The final, (the 8th), clock cycle is applied to the I/O clock pin. The on-chip sample-and-hold begins the hold function upon the high-to-low transition of this clock cycle. The hold function will continue for the next four internal system clock cycles, after which the holding function terminates and the conversion is performed during the next 32 system clock cycles, giving a total of 36 cycles. After the 8th I/O clock cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 36 internal system clock cycles to allow for the completion of the hold and conversion functions. $\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. If $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid high-to-low transition of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 internal system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

PRINCIPLES OF OPERATION

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the high-to-low transition of the 4th I/O clock cycle, the hold function does not begin until the high-to-low transition of the 8th I/O clock cycle, which should occur at the moment when the analog signal must be converted. The TLC548 and TLC549 will continue sampling the analog input until the high-to-low transition of the 8th I/O clock pulse. The control circuitry or software will then immediately lower the I/O clock signal and start the holding function to hold the analog signal at the desired point in time and start conversion.

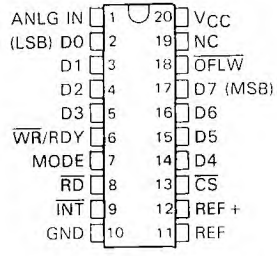
Detailed information on interfacing to the most popular microprocessor is readily available from Texas Instruments.

TLC0820A, TLC0820B, ADC0820B, ADC0820C
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTERS USING MODIFIED "FLASH" TECHNIQUES

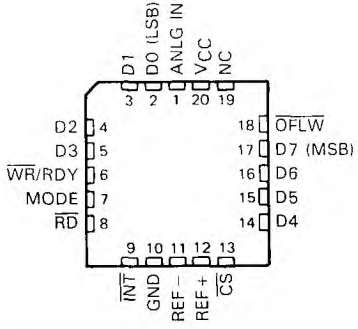
D2873, SEPTEMBER 1986–REVISED FEBRUARY 1989

- Advanced LinCMOS™ Silicon-Gate Technology
- 8-Bit Resolution
- Differential Reference Inputs
- Parallel Microprocessor Interface
- Conversion and Access Time Over Temperature Range
  - Write-Read Mode . . . 1.18 μs and 1.92 μs
  - Read Mode . . . 2.5 μs Max
- No External Clock or Oscillator Components Required
- On-Chip Track-and-Hold
- Low Power Consumption . . . 50 mW Typ
- Single 5-V Supply
- TLC0820B is Direct Replacement for National Semiconductor ADC0820B/BC and Analog Devices AD7820L/C/U; TLC0820A is Direct Replacement for National Semiconductor ADC0820C/CC and Analog Devices AD7820K/B/T

ALL TYPES . . DW OR N PACKAGE
TLC0820_M . . . J PACKAGE
(TOP VIEW)



TLC0820_M . . . FK PACKAGE
TLC0820_I, TLC0820_C . . . FN PACKAGE
ADC0820_CI, ADC0820_C . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC0820A, TLC0820B, ADC0820B, and ADC0820C are Advanced LinCMOS™ 8-bit analog-to-digital converters each consisting of two 4-bit "flash" converters, a 4-bit digital-to-analog converter, a summing (error) amplifier, control logic, and a result latch circuit. The modified "flash" technique allows low-power integrated circuitry to complete an 8-bit conversion in 1.18 μs over temperature. The on-chip track-and-hold circuit has a 100 ns sample window and allows these devices to convert continuous analog signals having slew rates of up to 100 mV/μs without external sampling components. TTL-compatible three-state output drivers and two modes of operation allow interfacing to a variety of microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C. See Available Options.

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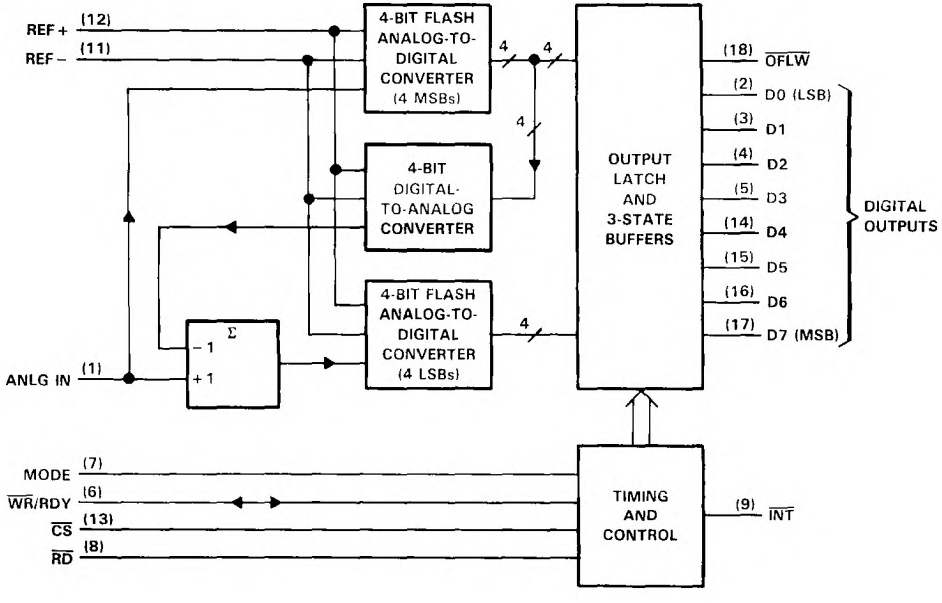
AVAILABLE OPTIONS

SYMBOLIZATION†		OPERATING TEMPERATURE RANGE	TOTAL UNADJUSTED ERROR
DEVICE	PACKAGE SUFFIX		
TLC0820AC	DW, FN, N	0°C to 70°C	±1 LSB
TLC0820AI	DW, FN, N	−40°C to 85°C	±1 LSB
TLC0820AM	DW, FK, J, N	−55°C to 125°C	±1 LSB
TLC0820BC	DW, FN, N	0°C to 70°C	±0.5 LSB
TLC0820BI	DW, FN, N	−40°C to 85°C	±0.5 LSB
TLC0820BM	DW, FK, J, N	−55°C to 125°C	±0.5 LSB
ADC0820BC	DW, FN, N	0°C to 70°C	±0.5 LSB
ADC0820BCI	DW, FN, N	−40°C to 85°C	±0.5 LSB
ADC0820CC	DW, FN, N	0°C to 70°C	±1 LSB
ADC0820CCI	DW, FN, N	−40°C to 85°C	±1 LSB

†In many instances, these ICs may have both TLC0820 and ADC0820 labeling on the package

functional block diagram



PIN NAME	PIN NUMBER	DESCRIPTION
ANLG IN	1	Analog input
$\overline{CS}$	13	This input must be low in order for $\overline{RD}$ or $\overline{WR}$ to be recognized by the ADC.
D0	2	Three-state data output, bit 1 (LSB)
D1	3	Three-state data output, bit 2
D2	4	Three-state data output, bit 3
D3	5	Three-state data output, bit 4
D4	14	Three-state data output, bit 5
D5	15	Three-state data output, bit 6
D6	16	Three-state data output, bit 7
D7	17	Three-state data output, bit 8 (MSB)
GND	10	Ground
$\overline{INT}$	9	In the WRITE-READ mode, the interrupt output, $\overline{INT}$, going low indicates that the internal count-down delay time, $t_{d(int)}$, is complete and the data result is in the output latch. $t_{d(int)}$ is typically 800 ns starting after the rising edge of the $\overline{WR}$ input (see operating characteristics and Figure 3). If $\overline{RD}$ goes low prior to the end of $t_{d(int)}$, $\overline{INT}$ goes low at the end of t_{dRIL} and the conversion results are available sooner (see Figure 2). $\overline{INT}$ is reset by the rising edge of either $\overline{RD}$ or $\overline{CS}$.
MODE	7	Mode-selection input. It is internally tied to GND through a 50-μA current source, which acts like a pull-down resistor. READ mode: Occurs when this input is low. WRITE-READ mode: Occurs when this input is high.
NC	19	No internal connection
$\overline{OFLW}$	18	Normally the $\overline{OFLW}$ output is a logical high. However, if the analog input is higher than the V_{REF+}, $\overline{OFLW}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to improve resolution (9 or 10-bits).
$\overline{RD}$	8	In the WRITE-READ mode with $\overline{CS}$ low, the 3-state data outputs D0 through D7 are activated when $\overline{RD}$ goes low. $\overline{RD}$ can also be used to increase the conversion speed by reading data prior to the end of the internal count-down delay time. As a result, the data transferred to the output latch is latched after the falling edge of $\overline{RD}$. In the READ mode with $\overline{CS}$ low, the conversion starts with $\overline{RD}$ going low. $\overline{RD}$ also enables the three-state data outputs upon completion of the conversion. The RDY output going into the high-impedance state and $\overline{INT}$ going low indicates completion of the conversion.
REF −	11	This input voltage is placed on the bottom of the resistor ladder.
REF +	12	This input voltage is placed on the top of the resistor ladder.
V_{CC}	20	Power supply voltage
$\overline{WR}$/RDY	6	In the WRITE-READ mode with $\overline{CS}$ low, the conversion is started on the falling edge of the $\overline{WR}$ input signal. The result of the conversion is strobed into the output latch after the internal count-down delay time, $t_{d(int)}$, provided that the $\overline{RD}$ input does not go low prior to this time. $t_{d(int)}$ is approximately 800 ns. In the READ mode, RDY (an open-drain output) will go low after the falling edge of $\overline{CS}$, and will go into the high-impedance state when the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TLC0820_M	TLC0820_I ADC0820_CI	TLC0820_C ADC0820_C	UNIT
Supply voltage, V_{CC} (see Note 1)	10	10	10	V
Input voltage range, all inputs (see Note 1)	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	V
Output voltage range, all outputs (see Note 1)	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	−0.2 to V_{CC}+0.2	V
Operating free-air temperature range	−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260			°C
Case temperature for 10 seconds: FN package		260	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260	260	260	°C

NOTE 1: All voltages are with respect to network ground terminal, pin 10.

recommended operating conditions

			TLC0820_M			TLC0820_I ADC0820_CI			TLC0820_C ADC0820_C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	8	4.5	5	8	4.5	5	8	V
Analog input voltage			−0.1		V_{CC}+0.1	−0.1		V_{CC}+0.1	−0.1		V_{CC}+0.1	V
Positive reference voltage, V_{REF+}			V_{REF-}		V_{CC}	V_{REF-}		V_{CC}	V_{REF-}		V_{CC}	V
Negative reference voltage, V_{REF-}			GND		V_{REF+}	GND		V_{REF+}	GND		V_{REF+}	V
High-level input voltage, V_{IH}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$ MODE	2 3.5			2 3.5			2 3.5			V
Low-level input voltage, V_{IL}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$ MODE			0.8 1.5			0.8 1.5			0.8 1.5	V
Delay to next conversion, $t_{d(NC)}$ (see Figures 1, 2, 3, and 4)			500			500			500			ns
Delay time from $\overline{WR}$ to $\overline{RD}$ in write-read mode, t_{dWR} (see Figure 2)			0.4			0.4			0.4			μs
Write-pulse duration in write-read mode, t_{wW} (see Figures 2, 3, and 4)			0.5		50	0.5		50	0.5		50	μs
Operating free-air temperature, T_A			−55		125	−40		85	0		70	°C

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electrical characteristics at specified operating free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Any D, $\overline{INT}$, or $\overline{OFLW}$	V_{CC} = 4.75 V, I_{OH} = −360 μA	Full range	2.4			V
			V_{CC} = 4.75 V, I_{OH} = −10 μA	Full range	4.5			
				25°C	4.6			
V_{OL}	Low-level output voltage	Any D, $\overline{OFLW}$, $\overline{INT}$, or $\overline{WR}$/RDY	V_{CC} = 5.25 V, I_{OL} = 1.6 mA	Full range			0.4	V
				25°C			0.34	
I_{IH}	High-level input current	$\overline{CS}$ or $\overline{RD}$	V_{IH} = 5 V	Full range		0.005	1	μA
		$\overline{WR}$/RDY		Full range			3	
				25°C		0.1	0.3	
		MODE		Full range			200	
				25°C		50	170	
I_{IL}	Low-level input current	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$, or MODE	V_{IL} = 0	Full range		−0.005	−1	μA
I_{OZ}	Off-state (high-impedance state) output current	Any D or $\overline{WR}$/RDY	V_O = 5 V	Full range			3	μA
				25°C		0.1	0.3	
			V_O = 0	Full range			−3	
				25°C		−0.1	−0.3	
I_I	Analog input current		$\overline{CS}$ at 5 V, V_I = 5 V	Full range			3	μA
				25°C			0.3	
			$\overline{CS}$ at 5 V, V_I = 0	Full range			−3	
				25°C			−0.3	
I_{OS}	Short-circuit output current	Any D, $\overline{OFLW}$, $\overline{INT}$, or $\overline{WR}$/RDY	V_O = 5 V	Full range	7			mA
				25°C	8.4	14		
		Any D or $\overline{OFLW}$	V_O = 0	Full range	−6			
				25°C	−7.2	−12		
		$\overline{INT}$		Full range	−4.5			
				25°C	−5.3	−9		
R_{ref}	Reference resistance			Full range	1.25		6	kΩ
				25°C	1 4	2 3	5.3	
I_{CC}	Supply current		$\overline{CS}$, $\overline{WR}$/RDY, and $\overline{RD}$ at 0 V	Full range			15	mA
				25°C		7.5	13	
C_i	Input capacitance	Any digital		Full range		5		pF
		ANLG IN				45		
C_o	Output capacitance	Any digital		Full range			5	pF

†All typical values are at T_A = 25°C.

operating characteristics, V_{CC} = 5 V, V_{REF+} = 5 V, V_{REF-} = 0, $t_r = t_f$ = 20 ns, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC0820B ADC0820B			TLC0820A ADC0820C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVS}	Supply voltage sensitivity	V_{CC} = 5 V ± 5%, T_A = MIN to MAX			±1/16	±1/4		±1/16	±1/4	LSB
	Total unadjusted error†	MODE pin at 0 V, T_A = MIN to MAX				1/2			1	LSB
t_{convR}	Read mode conversion time	MODE pin at 0 V, See Figure 1			1.6	2.5		1.6	2.5	μs
$t_{d(int)}$	Internal count-down delay time	MODE pin at 5 V, See Figures 3 and 4	C_L = 50 pF,		800	1300		800	1300	ns
t_{aR}	Access time from $\overline{RD}$↓	MODE pin at 0 V, See Figure 1			t_{convR} +20	t_{convR} +50		t_{convR} +20	t_{convR} +50	ns
t_{aR1}	Access time from $\overline{RD}$↓	MODE pin at 5 V, $t_{dWR} < t_{d(int)}$, See Figure 2	C_L = 15 pF		190	280		190	280	ns
			C_L = 100 pF		210	320		210	320	
t_{aR2}	Access time from $\overline{RD}$↓	MODE pin at 5 V, $t_{dWR} > t_{d(int)}$ See Figure 3	C_L = 15 pF		70	120		70	120	ns
			C_L = 100 pF		90	150		90	150	
t_{aINT}	Access time from $\overline{INT}$↓	MODE pin at 5 V, See Figure 4			20	50		20	50	ns
t_{dis}	Disable time from $\overline{RD}$↑	R_L = 1 kΩ, See Figures 1, 2, 3, and 5	C_L = 10 pF,		70	95		70	95	ns
t_{dRDY}	Delay time from $\overline{CS}$↓ to RDY↓	MODE pin at 0 V, See Figure 1	C_L = 50 pF,		50	100		50	100	ns
t_{dRIH}	Delay time from $\overline{RD}$↑ to $\overline{INT}$↑	C_L = 50 pF, See Figures 1, 2, and 3			125	225		125	225	ns
t_{dRIL}	Delay time from $\overline{RD}$↓ to $\overline{INT}$↓	MODE pin at 5 V, Figure 2	$t_{dWR} < t_{d(int)}$,		200	290		200	290	ns
t_{dWIH}	Delay time from $\overline{WR}$↑ to $\overline{INT}$↑	E pin at 5 V, See Figure 4	C_L = 50 pF,		175	270		175	270	ns
	Slew rate tracking				0.1			0.1		V/μs

† Total unadjusted error includes offset, full-scale, and linearity errors.

PARAMETER MEASUREMENT INFORMATION

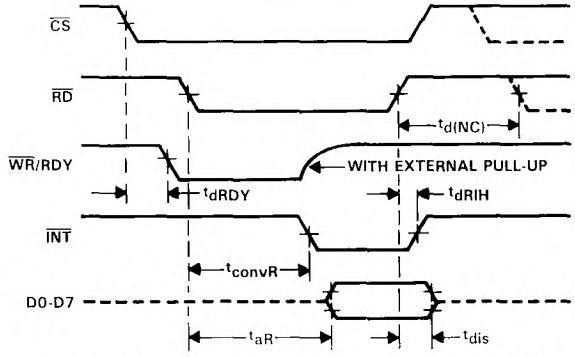


FIGURE 1. READ MODE WAVEFORMS (MODE PIN LOW)

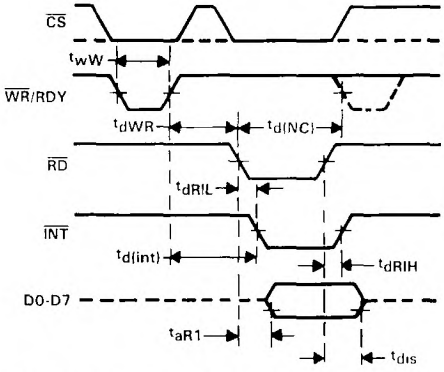


FIGURE 2. WRITE-READ MODE WAVEFORMS
[MODE PIN HIGH AND $t_{dWR} < t_{d(int)}$]

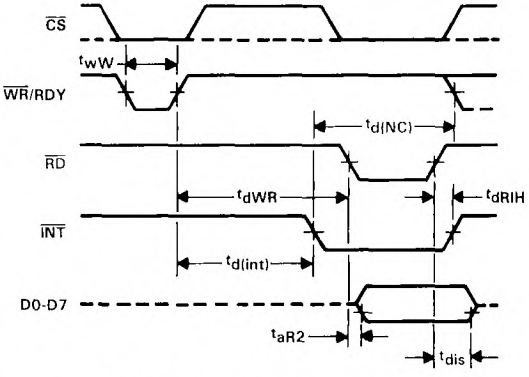


FIGURE 3. WRITE-READ WAVEFORMS
[MODE PIN HIGH AND $t_{dWR} > t_{d(int)}$]

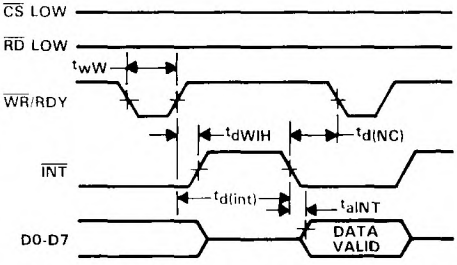


FIGURE 4. WRITE-READ MODE WAVEFORMS
(STAND-ALONE OPERATION, MODE PIN HIGH, AND RD LOW)

PARAMETER MEASUREMENT INFORMATION

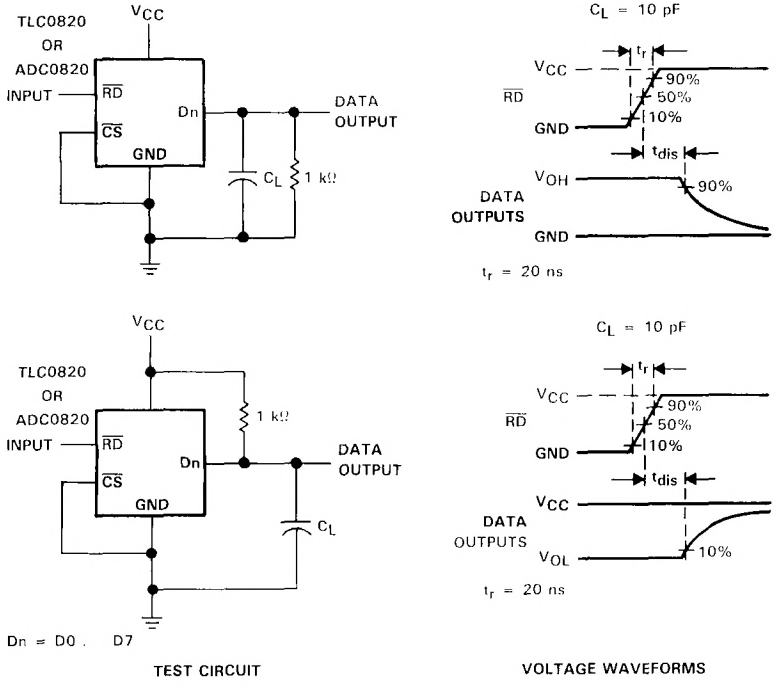


FIGURE 5. TEST CIRCUIT AND VOLTAGE WAVEFORMS

PRINCIPLES OF OPERATION

The TLC0820A, TLC0820B, ADC0820B and ADC0820C each employ a combination of "sampled-data" comparator techniques and "flash" techniques common to many high-speed converters. Two 4-bit "flash" analog-to-digital conversions are used to give a full 8-bit output.

The recommended analog input voltage range for conversion is -0.1 V to $V_{CC}+0.1$ V. Analog input signals that are less than V_{REF-} + ½ LSB or greater than V_{REF+} − ½ LSB convert to 00000000 or 11111111 respectively. The reference inputs are fully differential with common-mode limits defined by the supply rails. The reference input values define the full-scale range of the analog input. This allows the gain of the ADC to be varied for ratiometric conversion by changing the V_{REF+} and V_{REF-} voltages.

The device operates in two modes, read (only) and write-read, which are selected by the MODE pin (pin 7). The converter is set to the read (only) mode when pin 7 is low. In the read mode, the $\overline{WR}$/RDY pin is used as an output and is referred to as the "ready" pin. In this mode, a low on the "ready" pin while $\overline{CS}$ is low indicates that the device is busy. Conversion starts on the falling edge of $\overline{RD}$ and is completed no more than 2.5 μs later when $\overline{INT}$ falls and the "ready" pin returns to a high-impedance state. Data outputs also change from high-impedance to active states at this time. After the data is read, $\overline{RD}$ is taken high, $\overline{INT}$ returns high, and the data outputs return to their high-impedance states.

The converter is set to the write-read mode when pin 7 is high and $\overline{WR}$/RDY is referred to as the "write" pin. Taking $\overline{CS}$ and the "write" pin low selects the converter and initiates measurement of the input signal. Approximately 600 ns after the "write" pin returns high, the conversion is completed. Conversion starts on the rising edge of $\overline{WR}$/RDY in the write-read mode.

The high-order 4-bit "flash" ADC measures the input by means of 16 comparators operating simultaneously. A high precision 4-bit DAC then generates a discrete analog voltage from the result of that conversion. After a time delay, a second bank of comparators does a low-order conversion on the analog difference between the input level and the high-order DAC output. The results from each of these conversions enter an 8-bit latch and are output to the three-state buffers on the falling edge of $\overline{RD}$.

TYPICAL APPLICATION DATA

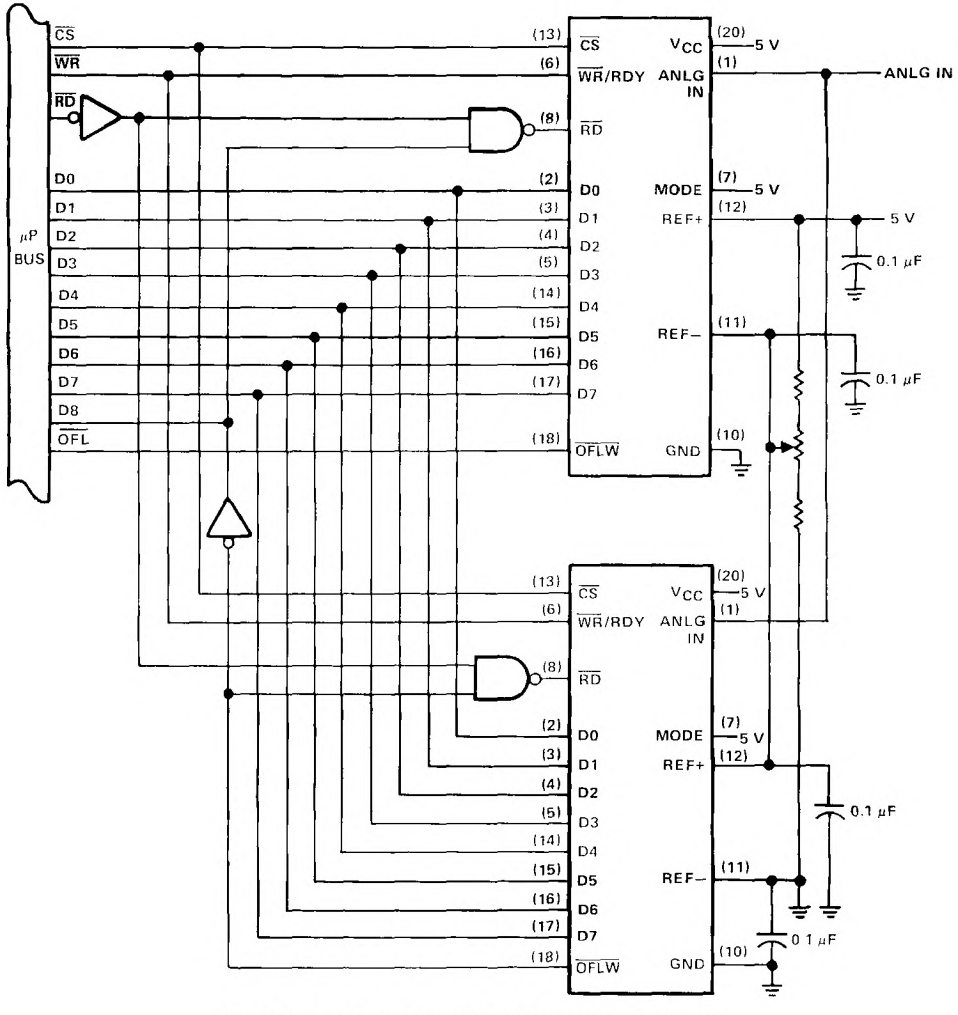
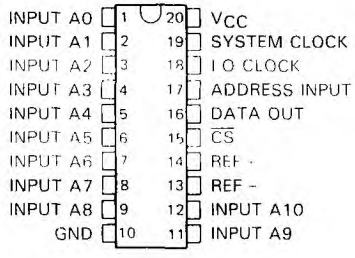


FIGURE 6. CONFIGURATION FOR 9-BIT RESOLUTION

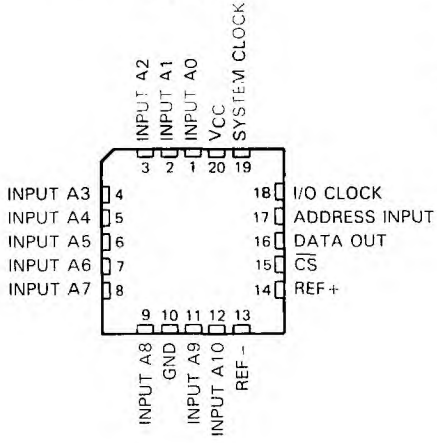
D2859, DECEMBER 1985 REVISED JANUARY 1988

- LinCMOS™ Technology
- 10-Bit Resolution A/D Converter
- Microprocessor Peripheral or Stand-Alone Operation
- On-Chip 12-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . .
  TLC1540: ±0.5 LSB Max
  TLC1541: ±1.0 LSB Max
- Pinout and Control Signals Compatible with TLC540 and TLC549 Families of 8-Bit A/D Converters

J OR N DUAL-IN LINE PACKAGE
(TOP VIEW)



FK OR FN CHIP CARRIER PACKAGE
(TOP VIEW)



TYPICAL PERFORMANCE	
Channel Acquisition Sample Time	5.5 μs
Conversion Time	21 μs
Samples per Second	32×10^3
Power Dissipation	6 mW

description

The TLC1540 and TLC1541 are LinCMOS™ A/D peripherals built around a 10-bit, switched-capacitor, successive-approximation, A/D converter. They are designed for serial interface to a microprocessor or peripheral via a three-state output with up to four control inputs (including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input). A 2.1-megahertz system clock for the TLC1540 and TLC1541, with a design that includes simultaneous read/write operation, allows high-speed data transfers and sample rates of up to 32,258 samples per second. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The converters incorporated in the TLC1540 and TLC1541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows guaranteed low-error conversion (±0.5 LSB for the TLC1540, ±1 LSB for the TLC1541) in 21 microseconds over the full operating temperature range.

The TLC1540 and the TLC1541 are available in FK, FN, J, and N packages. The M-suffix versions are characterized for operation from −55°C to 125°C. The I-suffix versions are characterized for operation from −40°C to 85°C.

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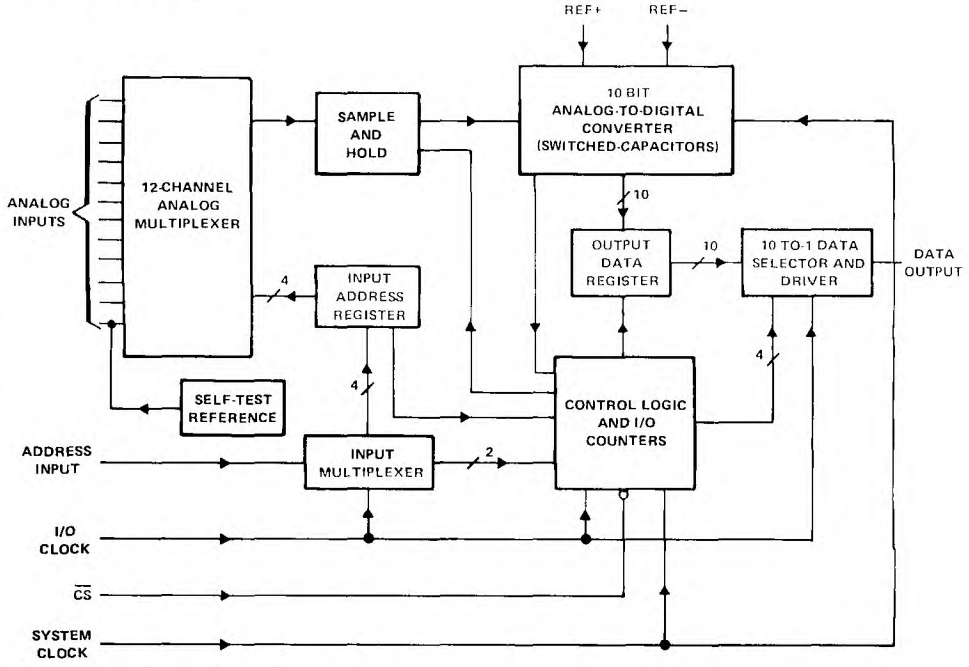
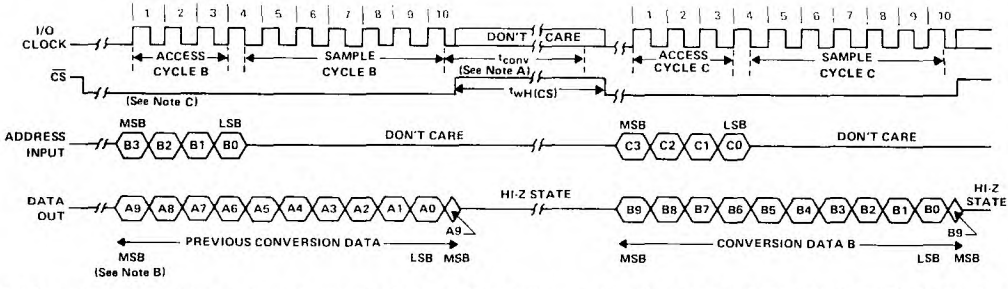
functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 44 System Clock periods, is initiated on the 10th falling edge of the I/O Clock↓ after CS↓ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, the I/O Clock must remain low for at least 44 System Clock cycles to allow conversion to be completed.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining nine bits (A8-A0) will be clocked out on the first nine I/O Clock falling edges.

C To minimize errors caused by noise at the CS input, the internal circuitry waits for three System Clock cycles (or less) after a chip-select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

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absolute *maximum* ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range (any input)	−0.3 V to V_{CC} + 0.3 V
Output voltage range	−0.3 V to V_{CC} + 0.3 V
Peak input current range (any input)	±10 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range: TLC1540I, TLC1541I	−40°C to 85°C
TLC1540M, TLC1541M	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: N package	260°C

NOTE 1: All voltage values are with respect to digital ground with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

			TLC1540, TLC1541			UNIT
			MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)			−0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	V
High-level control input voltage, V_{IH}			2			V
Low-level control input voltage, V_{IL}					0.8	V
Setup time, address bits before I/O CLK↑, $t_{su(A)}$			400			ns
Hold time, address bits after I/O CLK↑, $t_{h(A)}$			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3)			3			System clock cycles
$\overline{CS}$ high during conversion, $t_{wH(CS)}$			44			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0		1.1	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$		2.1	MHz
System clock high, t_{wH}			210			ns
System clock low, t_{wL}			190			ns
Input/Output clock high, $t_{wH(I/O)}$			404			ns
Input/Output clock low, $t_{wL(I/O)}$			404			ns
Clock transition time (see Note 4)	System	$f_{CLK(SYS)} \le 1048$ kHz			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40	
Operating free-air temperature, T_A		TLC1540M, TLC1541M	−55		125	°C
		TLC1540I, TLC1541I	−40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 volts.

3. To minimize errors caused by noise at the chip select input, the internal circuitry waits for three System Clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in an address until the minimum chip select setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 microseconds for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)}$ = 1.1 MHz, $f_{CLK(SYS)}$ = 2.1 MHz

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 16)		V_{CC} = 4.75 V,	I_{OH} = 360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		V_I = V_{CC}			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
I_{CC} + I_{REF}	Supply and reference current		V_{REF+} = V_{CC},	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

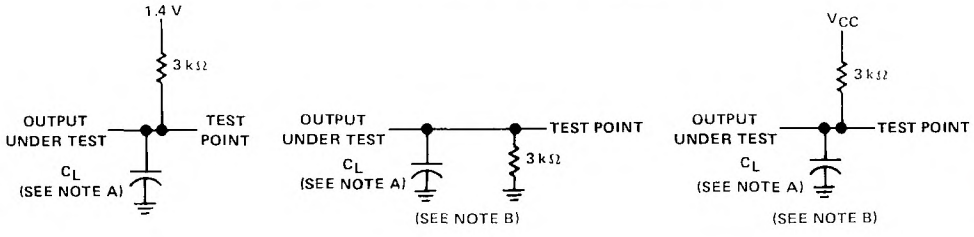
operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{REF+} = 4.75 V to 5.5 V, $f_{CLK(I/O)}$ = 1.1 MHz, $f_{CLK(SYS)}$ = 2.1 MHz

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
	Linearity error	TLC1540	See Note 5		±0.5	LSB
		TLC1541			±1	
	Zero error	TLC1540	See Notes 2 and 6		±0.5	LSB
		TLC1541			±1	
	Full-scale error	TLC1540	See Notes 2 and 6		±0.5	LSB
		TLC1541			±1	
	Total unadjusted error	TLC1540	See Note 7		±0.5	LSB
		TLC1541			±1	
	Self-test output code		Input A11 address = 1011 (See Note 8)	0111110100 (500)	1000001100 (524)	
t_{conv}	Conversion time		See Operating Sequence		21	μs
	Total access and conversion time		See Operating Sequence		31	μs
t_{acq}	Channel acquisition time (sample cycle)		See Operating Sequence		6	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓			10		ns
t_d	Delay time, I/O clock↓ to data output valid		See Parameter Measurement Information		400	ns
t_{en}	Output enable time				150	ns
t_{dis}	Output disable time				150	ns
$t_{r(bus)}$	Data bus rise time				300	ns
$t_{f(bus)}$	Data bus fall time				300	ns

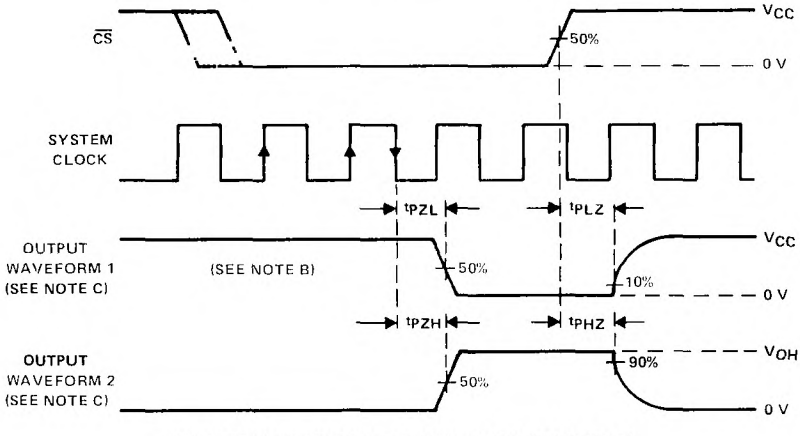
NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all "1"s (11111111), while input voltages less than that applied to REF− convert to all"0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 volts.

5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error comprises linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The A11 analog input signal is internally generated and is used for test purposes.

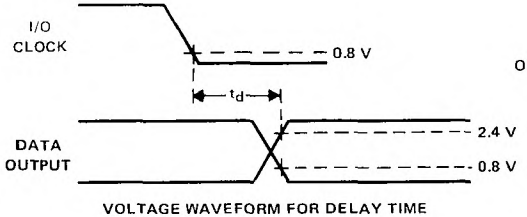
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR t_d, t_r, AND t_f | LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ} | LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME

VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES A. C_L 50 pF
B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control

principles of operation

The TLC1540 and TLC1541 are complete data acquisition systems on single chips. Each includes such functions as sample-and-hold, 10-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs; Chip Select ($\overline{CS}$), Address Input, I/O Clock, and System Clock. These control inputs and a TTL-compatible three-state output are intended for serial communications with a microprocessor or microcomputer. The TLC1540 and TLC1541 can complete conversions in a maximum of 21 microseconds, while complete input-conversion-output cycles can be repeated at a maximum of 31 microseconds.

The System and I/O Clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the System Clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O Clock. The System Clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the Data Output pin is in a three-state condition and the Address Input and I/O Clock pins are disabled. This feature allows each of these pins, with the exception of the $\overline{CS}$ pin, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC1540/1541 devices are used. In this way, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the System Clock after a low $\overline{CS}$ transition, before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result will automatically appear on the Data Out pin.
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of the I/O Clock. The MSB of the address is shifted in first. The negative edges of these four I/O Clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Five clock cycles are then applied to the I/O pin and the sixth, seventh, eighth, ninth, and tenth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final tenth clock cycle is applied to the I/O Clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 44 System Clock cycles. After this final I/O Clock cycle, $\overline{CS}$ must go high or the I/O Clock must remain low for at least 44 System Clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 44 System Clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the System and I/O Clock pins together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O Clock. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the "conversion crunching" circuitry.
2. The device will recognize a $\overline{CS}$ low transition only when the $\overline{CS}$ input changes and subsequently the System Clock pin receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O Clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the eighth I/O Clock that has been recognized by the device, so that a $\overline{CS}$ low level will be recognized upon the lowering of the tenth I/O Clock signal that is recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O Clock pulses and will shift in an erroneous address.

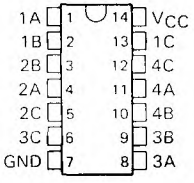
For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample-and-hold *begins* sampling upon the negative edge of the fourth I/O Clock cycle, the hold function is not initiated until the negative edge of the tenth I/O Clock cycle. Thus, the control circuitry can leave the I/O Clock signal in its high state during the tenth I/O Clock cycle until the moment at which the analog signal must be converted. The TLC1540/TLC1541 will continue sampling the analog input until the tenth falling edge of the I/O Clock. The control circuitry or software will then immediately lower the I/O Clock signal and hold the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

D2922, JANUARY 1986–REVISED OCTOBER 1988

- High Degree of Linearity
- High On-Off Output Voltage Ratio
- Low Crosstalk Between Switches
- Low On-State Impedance . . . 50 Ω Typ at V_{CC} = 9 V
- Individual Switch Controls
- Extremely Low Input Current

TLC4016M . . . J OR N PACKAGE
TLC4016I . . . D OR N PACKAGE
(TOP VIEW)



description

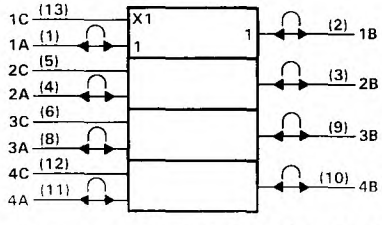
The TLC4016 is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 12 V peak to be transmitted in either direction.

Each switch section has its own enable input control. A high-level voltage applied to this control terminal turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

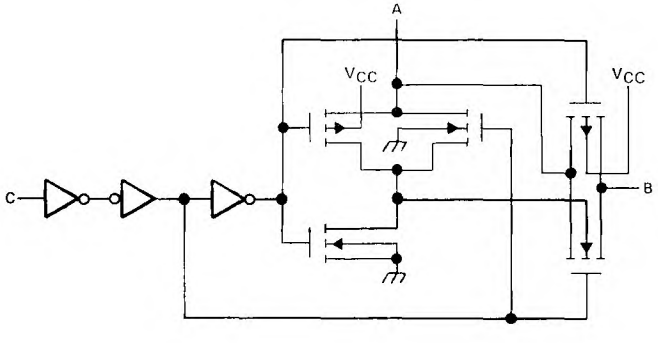
The TLC4016M is characterized for operation from −55°C to 125°C, and the TLC4016I is characterized from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1) . . . . . −0.5 V to 15 V
Control-input diode current ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
I/O port diode current ($V_I < 0$ or $V_{I/O} > V_{CC}$) . . . . . ±20 mA
On-state switch current ($V_{I/O} = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Continuous total dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range: TLC4016M . . . . . −55°C to 125°C
TLC4016I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltages are with respect to ground unless otherwise specified.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2[1]	5	12	V
I/O port voltage, $V_{I/O}$		0		V_{CC}	V
High-level input voltage, V_{IH}	V_{CC} = 2 V	1.5		V_{CC}	V
	V_{CC} = 4.5 V	3.15		V_{CC}	
	V_{CC} = 9 V	6.3		V_{CC}	
	V_{CC} = 12 V	8.4		V_{CC}	
Low-level input voltage, V_{IL}	V_{CC} = 2 V	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	
	V_{CC} = 9 V	0		1.8	
	V_{CC} = 12 V	0		2.4	
Input rise time, t_r	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Input fall time, t_f	V_{CC} = 2 V			1	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Operating free-air temperature, T_A	TLC4016M	−55		125	°C
	TLC4016I	−40		85	

[1] With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	V_{CC}	TLC4016M			TLC4016I			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
r_{Son}	On-state switch resistance		I_S = 1 mA, V_A = 0 to V_{CC}, See Figure 1	4.5 V					100	200	Ω
				9 V		30	120		50	105	
				12 V		30	100		30	85	
			I_S = 1 mA, V_A = 0 or V_{CC}, See Figure 1	2 V		120	240		120	215	
				4.5 V		50	120		50	100	
				9 V		35	80		35	75	
				12 V		20	70		20	60	
	On-state switch resistance matching		V_A = 0 to V_{CC}, See Figure 1	4.5 V		10	20		10	20	Ω
				9 V		5	15		5	15	
				12 V		5	15		5	15	
I_I	Control input current		V_I = 0 or V_{CC}	2 V to 6 V			±1			±1	μA
			V_I = 0 or V_{CC}, T_A = 25°C				±0.1			±0.1	
I_{Soff}	Off-state switch leakage current		V_S = ±V_{CC}, See Figure 2	5.5 V		±10	±600		±10	±600	nA
				9 V		±15	±800		±15	±800	
				12 V		±20	±1000		±20	±1000	
I_{Son}	On-state switch leakage current		V_A = 0 or V_{CC}, See Figure 3	5.5 V		±10	±150		±10	±150	nA
				9 V		±15	±200		±15	±200	
				12 V		±20	±300		±20	±300	
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	5.5 V		2	40		2	20	μA
				9 V		8	160		8	80	
				12 V		16	320		16	160	
C_i	Input capacitance	A or B		2 V to 12 V		15			15		pF
		C				5	10		5	10	
C_f	Feedthrough capacitance	A to B	V_I = 0	2 V to 12 V		5			5		pF

†All typical values are at T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TLC4016M			TLC4016I			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Propagation delay time, A to B or B to A	See Figure 4	2 V		25	75		25	62	ns
			4.5 V		5	15		5	13	
			9 V		4	14		4	12	
			12 V		3	13		3	11	
t_{on}	Switch turn-on time	R_L = 1 kΩ, See Figures 5 and 6	2 V		32	150		32	125	ns
			4.5 V		8	30		8	25	
			9 V		6	18		6	15	
			12 V		5	15		5	13	
t_{off}	Switch turn-off time	R_L = 1 kΩ, See Figures 5 and 6	2 V		45	252		45	210	ns
			4.5 V		15	54		15	45	
			9 V		10	48		10	40	
			12 V		8	45		8	38	
f_{co}	Switch cutoff frequency (channel loss = 3 dB)		4.5 V		100			100		MHz
			9 V		120			120		
$V_{OCF(PP)}$	Control feedthrough voltage to any switch, peak to peak	See Figure 7	4 5 V			350			350	mV
	Frequency at which crosstalk attenuation between any two switches equals 50 dB	See Figure 8	4 5 V		1			1		MHz

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

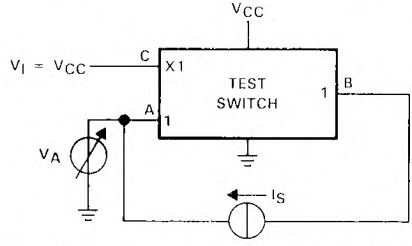
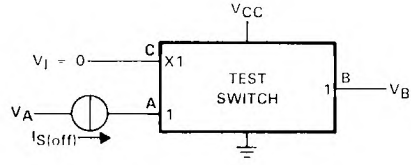


FIGURE 1. TEST CIRCUIT FOR ON-STATE RESISTANCE



$V_S = V_A - V_B$

CONDITION 1: V_A = 0, $V_B = V_{CC}$

CONDITION 2: $V_A = V_{CC}$, V_B = 0

FIGURE 2. TEST CIRCUIT FOR OFF-STATE SWITCH LEAKAGE CURRENT

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PARAMETER MEASUREMENT INFORMATION

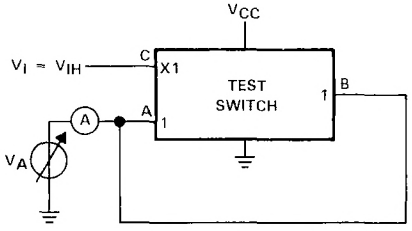
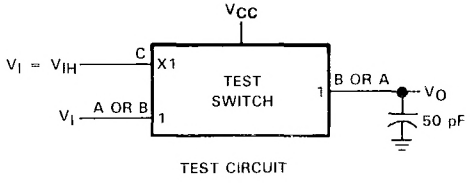
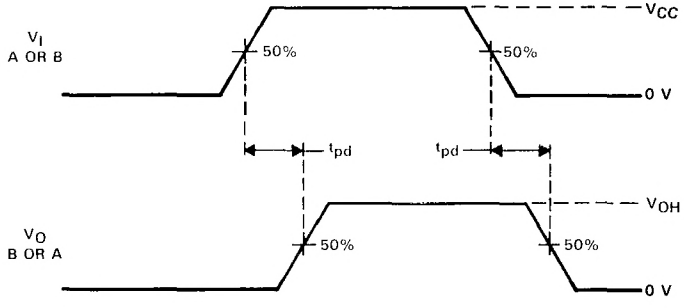


FIGURE 3. TEST CIRCUIT FOR ON-STATE SWITCH LEAKAGE CURRENT



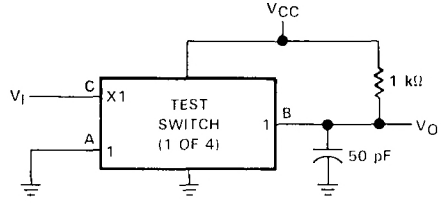
TEST CIRCUIT



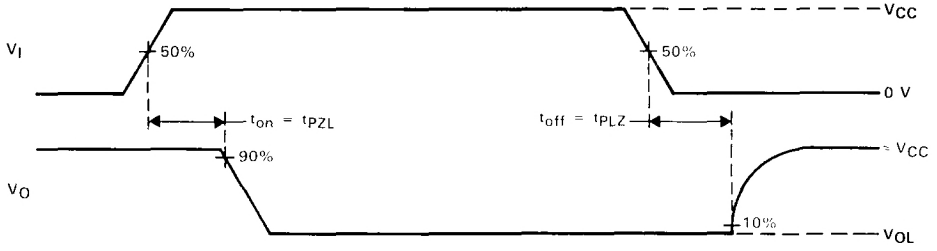
VOLTAGE WAVEFORMS

FIGURE 4. PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



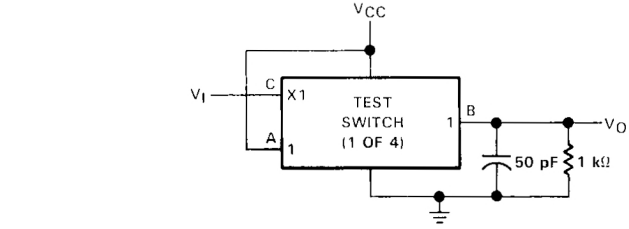
TEST CIRCUIT



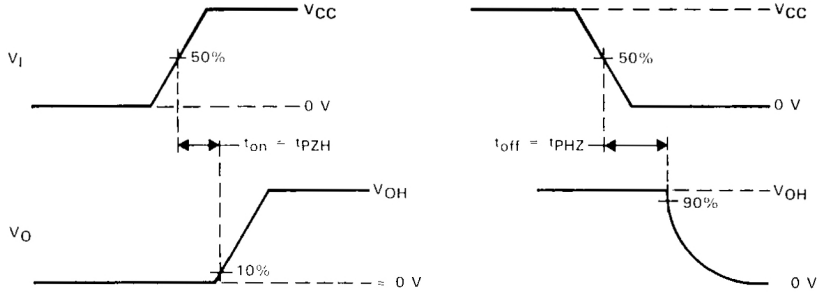
VOLTAGE WAVEFORMS

FIGURE 5. SWITCHING TIME (t_{PZL}, t_{PLZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 6. SWITCHING TIME (t_{PZH}, t_{PHZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION

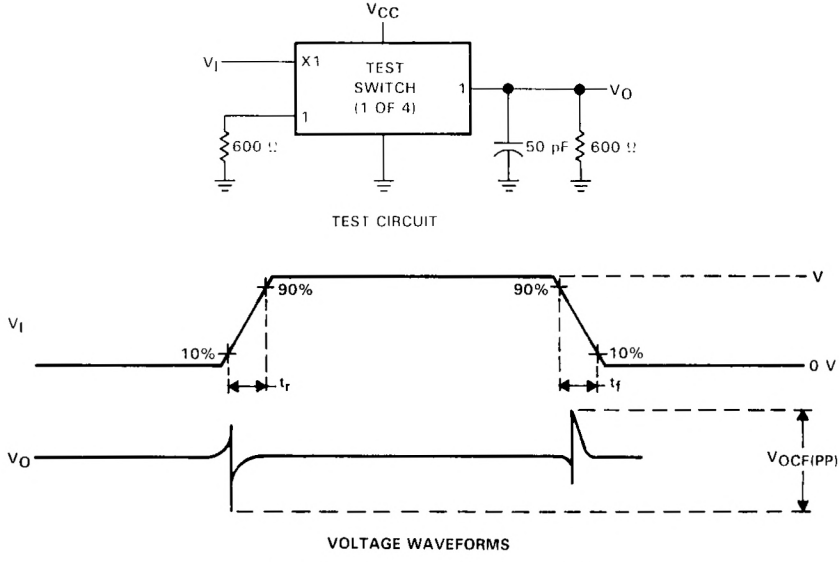
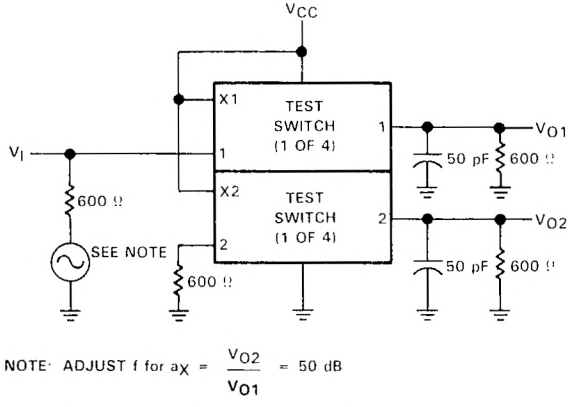


FIGURE 7. CONTROL FEEDTHROUGH VOLTAGE



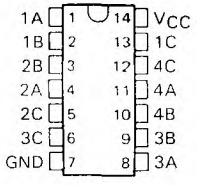
NOTE: ADJUST f for $a_X = \frac{V_{O2}}{V_{O1}} = 50$ dB

FIGURE 8. CROSSTALK BETWEEN ANY TWO SWITCHES, TEST CIRCUIT

D2922, JANUARY 1986 – REVISED OCTOBER 1988

- High Degree of Linearity
- High On-Off Output Voltage Ratio
- Low Crosstalk Between Switches
- Low On-State Impedance . . . 30 Ω Typ at V_{CC} = 12 V
- Individual Switch Controls
- Extremely Low Input Current
- Functionally Interchangeable with National Semiconductor MM54/74HC4066, Motorola MC54/74HC4066, and RCA CD4066A

TLC4066M . . . J OR N PACKAGE
TLC4066I . . . D OR N PACKAGE
(TOP VIEW)



description

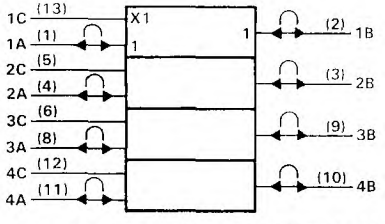
The TLC4066 is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 12 V peak to be transmitted in either direction.

Each switch section has its own enable input control. A high-level voltage applied to this control terminal turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

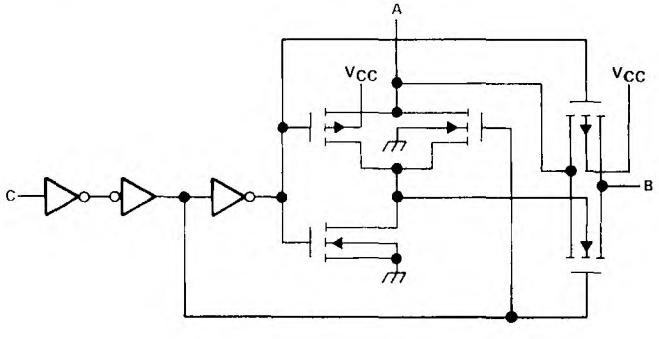
The TLC4066M is characterized for operation from −55°C to 125°C. The TLC4066I is characterized from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1) . . . . . −0.5 V to 15 V
Control-input diode current ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
I/O port diode current ($V_I < 0$ or $V_{I/O} > V_{CC}$) . . . . . ±20 mA
On-state switch current ($V_{I/O}$ = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Continuous total dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature: TLC4066M . . . . . −55°C to 125°C
TLC4066I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltages are with respect to ground unless otherwise specified.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2†	5	12	V
I/O port voltage, $V_{I/O}$		0		V_{CC}	V
High-level input voltage, V_{IH}	V_{CC} = 2 V	1.5		V_{CC}	V
	V_{CC} = 4.5 V	3.15		V_{CC}	
	V_{CC} = 9 V	6.3		V_{CC}	
	V_{CC} = 12 V	8.4		V_{CC}	
Low-level input voltage, V_{IL}	V_{CC} = 2 V	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	
	V_{CC} = 9 V	0		1.8	
	V_{CC} = 12 V	0		2.4	
Input rise time, t_r	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Input fall time, t_f	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Operating free-air temperature, T_A	TLC4066M	−55		125	°C
	TLC4066I	−40		85	

†With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	TLC4066M			TLC4066I			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
r_{Son}	On-state switch resistance		I_S = 1 mA, V_A = 0 to V_{CC}, See Figure 1	4.5 V		100	220		100	200	Ω
				9 V		50	110		50	105	
				12 V		30	90		30	85	
			I_S = 1 mA, V_A = 0 or V_{CC}, See Figure 1	2 V		120			120		
				4.5 V		50			50		
				9 V		35	80		35	75	
				12 V		20	70		20	60	
	On-state switch resistance matching		V_A = 0 to V_{CC}, See Figure 1	4.5 V		10	20		10	20	Ω
				9 V		5	15		5	15	
				12 V		5	15		5	15	
I_I	Control input current		V_I = 0 or V_{CC}	2 V or 6 V			±1			±1	μA
I_{Soff}	Off-state switch leakage current		V_S = ±V_{CC}, See Figure 2	5.5 V		±10	±600		±10	±600	nA
				9 V		±15	±		±15		
				12 V		±20	±		±20	±	
I_{Son}	On-state switch leakage current		V_A = 0 or V_{CC}, See Figure 3	5.5 V		±10	±150		±10	±150	nA
				9 V		±15	±		±15	±	
				12 V		±20	±		±20	±	
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	5.5 V		2	40		2	20	μA
				9 V		8	160		8	80	
				12 V		16	320		16	160	
C_i	Input capacitance	A or B		2 V to 12 V		15			15		pF
		C				5	10		5	10	
C_f	Feedthrough capacitance	A to B	V_I = 0	2 V to 12 V		5			5		pF

†All typical values are at T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TLC4066M			TLC4066I			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Propagation delay time, A to B or B to A	See Figure 4	2 V		25	75		15	30	ns
			4.5 V		5	15		5	13	
			9 V		4	12		4	10	
			12 V		3	13		3	11	
t_{on}	Switch turn-on time	R_L = 1 kΩ, See Figures 5 and 6	2 V		32	150		32	125	ns
			4.5 V		8	30		8	25	
			9 V		6	18		6	15	
			12 V		5	15		5	13	
t_{off}	Switch turn-off time	R_L = 1 kΩ, See Figures 5 and 6	2 V		45	252		45	210	ns
			4.5 V		15	54		15	45	
			9 V		10	48		10	40	
			12 V		8	45		8	38	
f_{co}	Switch cutoff frequency (channel loss = 3 dB)		4.5 V		100					MHz
			9 V		120			120		
$V_{OCF(PP)}$	Control feedthrough voltage to any switch, peak to peak	See Figure 7	4.5 V			350			350	mV
	Frequency at which crosstalk attenuation between any two switches equals 50 dB	See Figure 8	4.5 V		1			1		MHz

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

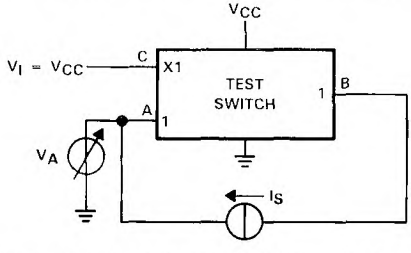
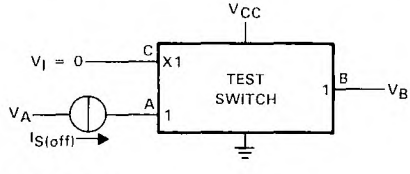


FIGURE 1. TEST CIRCUIT FOR ON-STATE RESISTANCE



$V_S = V_A - V_B$
CONDITION 1: V_A = 0, $V_B = V_{CC}$
CONDITION 2: $V_A = V_{CC}$, V_B = 0

FIGURE 2. TEST CIRCUIT FOR OFF-STATE SWITCH LEAKAGE CURRENT

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PARAMETER MEASUREMENT INFORMATION

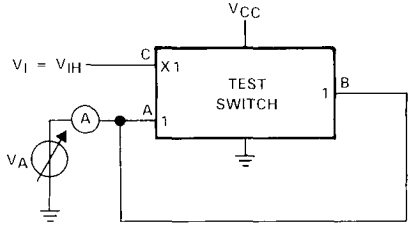
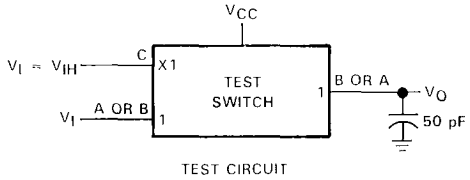
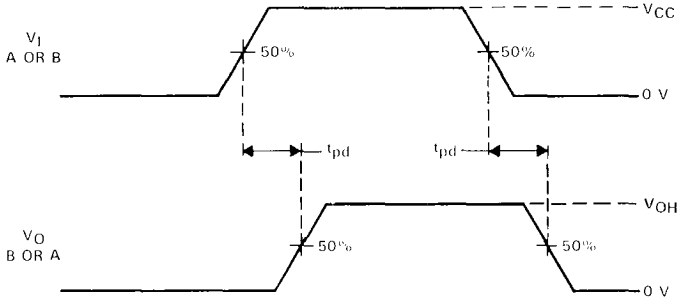


FIGURE 3. TEST CIRCUIT FOR ON-STATE SWITCH LEAKAGE CURRENT



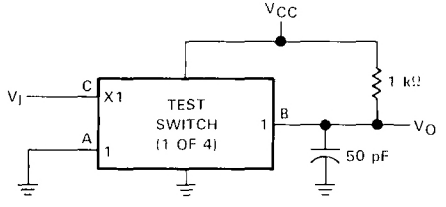
TEST CIRCUIT



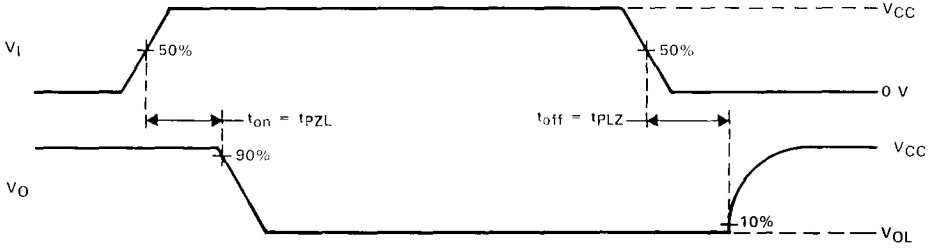
VOLTAGE WAVEFORMS

FIGURE 4. PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



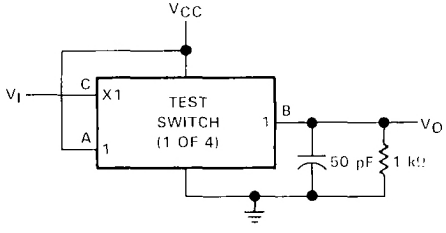
TEST CIRCUIT



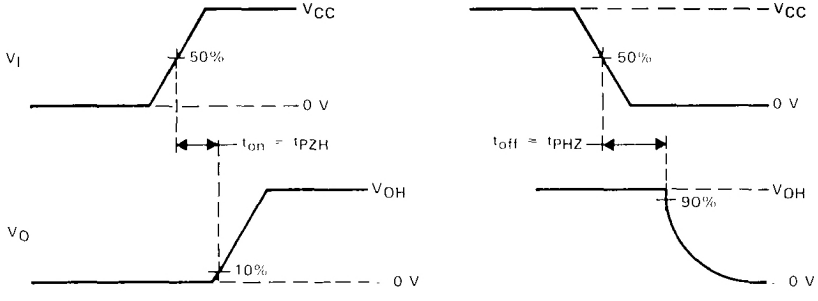
VOLTAGE WAVEFORMS

FIGURE 5. SWITCHING TIME (t_{PZL}, t_{PLZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 6. SWITCHING TIME (t_{PZH}, t_{PHZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION

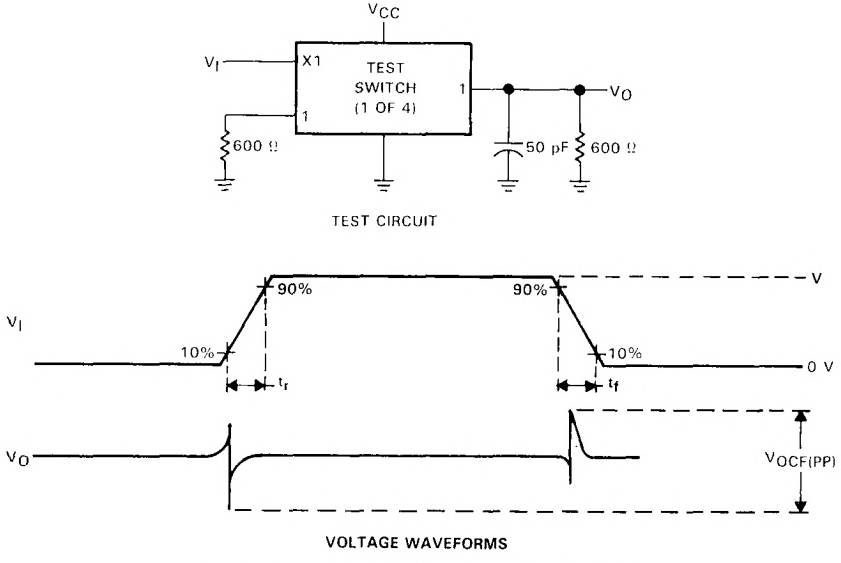
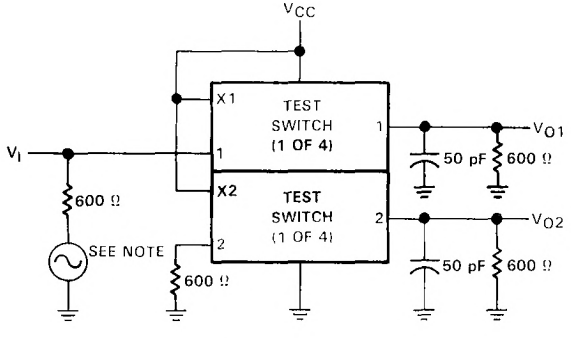


FIGURE 7. CONTROL FEEDTHROUGH VOLTAGE



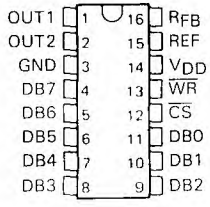
NOTE: ADJUST f for $a_X = \frac{V_{O2}}{V_{O1}} = 50$ dB.

FIGURE 8. CROSSTALK BETWEEN ANY TWO SWITCHES, TEST CIRCUIT

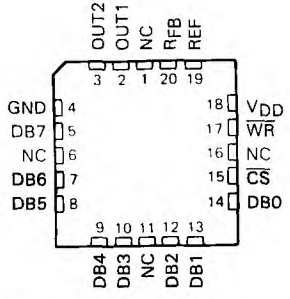
- Advanced LinCMOS™ Silicon-Gate Technology
- Easily Interfaced to Microprocessors
- On-Chip Data Latches
- Monotonic over the Entire A/D Conversion Range
- Segmented High-Order Bits Ensure Low-Glitch Output
- Designed to be Interchangeable with Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524
- Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	½ LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

D OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

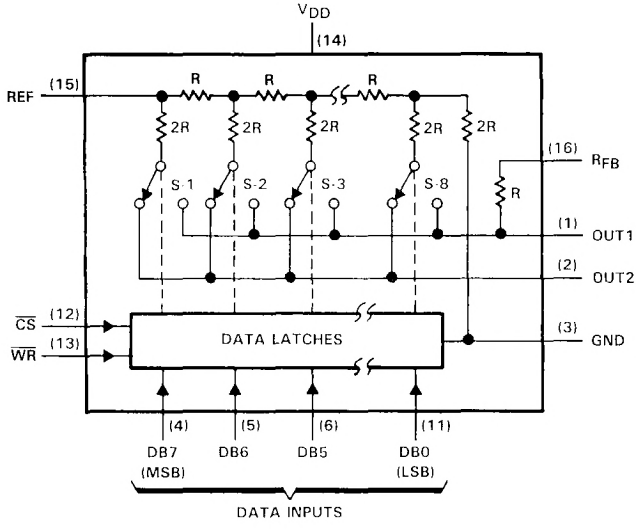
The TLC7524 is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The TLC7524 is an 8-bit multiplying DAC with input latches and with a load cycle similar to the "write" cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The TLC7524 provides accuracy to ½ LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 milliwatts typically.

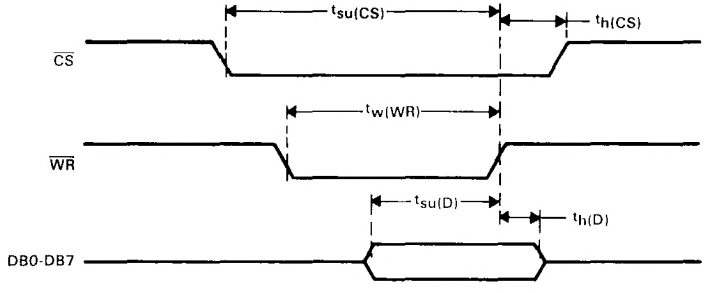
Featuring operation from a 5-V to 15-V single supply, the TLC7524 interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the TLC7524 an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7524I is characterized for operation from –25°C to 85°C, and the TLC7524C is characterized for operation from 0°C to 70°C.

functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} . . . . . −0.3 V to 16.5 V
Digital input voltage, V_I . . . . . −0.3 V to V_{DD} + 0.3 V
Reference voltage, V_{ref} . . . . . ±25 V
Peak digital input current, I_I . . . . . 10 μA
Operating free-air temperature range: TLC7524I . . . . . −25°C to 85°C
TLC7524C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

recommended operating conditions

		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN		MAX	MIN		MAX	
Supply voltage, V_{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
CS setup time, $t_{su(CS)}$		40			40			ns
CS hold time, $t_{h(CS)}$		0			0			ns
Data bus input setup time, $t_{su(D)}$		25			25			ns
Data bus input hold time, $t_{h(D)}$		10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		40			40			ns
Operating free-air temperature, T_A	TLC7524I	−25		85	−25		85	°C
	TLC7524C	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$			10			10	μA
I_{IL}	Low-level input current		V_I = 0			−10			−10	μA
I_{lkg}	Output leakage current	OUT1	DB0-DB7 at 0 V, $\overline{WR}$, $\overline{CS}$ at 0 V, V_{ref} = ±10 V			±400			±200	nA
		OUT2	DB0-DB7 at V_{DD}, $\overline{WR}$, $\overline{CS}$ at 0 V, V_{ref} = ±10 V			±400			±200	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH}min or V_{IL}max			1			2	mA
		Standby	DB0-DB7 at 0 V or V_{DD}			500			500	μA
k_{SVS}	Supply voltage sensitivity, $\Delta gain/\Delta V_{DD}$		ΔV_{DD} = ±10%		0.01	0.16		0.005	0.04	%FSR/%
C_i	Input capacitance, DB0-DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0			5			5	pF
C_o	Output capacitance	'1	DB0-DB7 at 0 V, $\overline{WR}$ and $\overline{CS}$ at 0 V			30			30	pF
		'2				120			120	
C_o	Output capacitance	OUT1	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V			120			120	pF
		OUT2				30			30	
	Reference input impedance (Pin 15 to GND)			5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = ±10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	TYP	MAX	MIN	TYP†	MAX	
Linearity error				±0.5			±0.5	
Gain error	See Note 1			±2.5				
Settling time (to ½ LSB)	See Note 2			100				ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80			80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100-kHz sinewave) $\overline{WR}$ and $\overline{CS}$ at 0 V, DB0-DB7 at 0 V			0.5			0.5	%FSR
Temperature coefficient of gain	T_A = 25°C to MAX		±0.004			±0.001		%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} – 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

principles of operation

The TLC7524 is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the TLC7524 D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the TLC7524 analog output responds to the data activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The TLC7524 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

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principles of operation (continued)

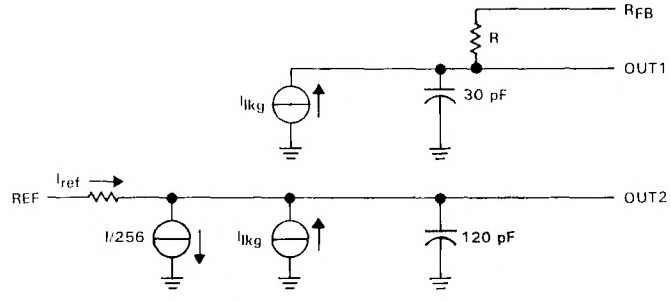

FIGURE 1. TLC7524 EQUIVALENT CIRCUIT WITH ALL DIGITAL INPUTS LOW

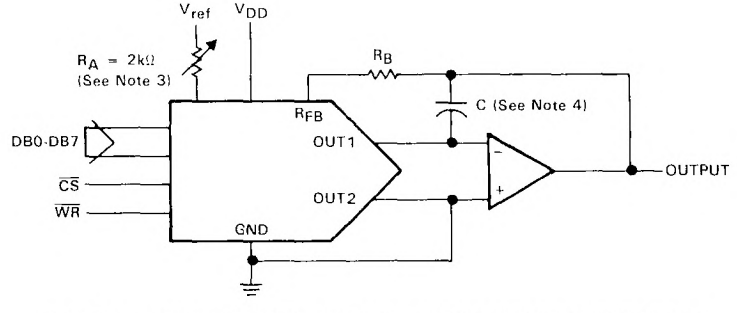

FIGURE 2. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

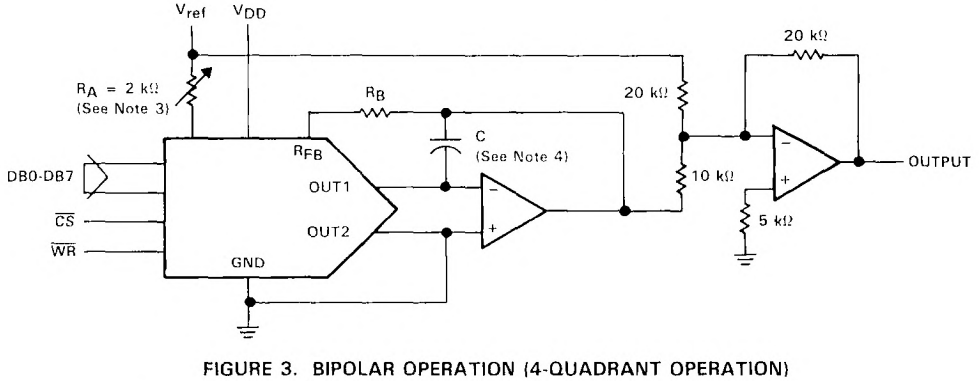

FIGURE 3. BIPOLAR OPERATION (4-QUADRANT OPERATION)

NOTES: 3. R_A and R_B used only if gain adjustment is required.
4. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

principles of operation (continued)

TABLE 1. UNIPOLAR BINARY CODE

DIGITAL INPUT (SEE NOTE 5) MSB LSB	ANALOG OUTPUT
11111111	$-V_{ref}$ (255/256)
10000001	$-V_{ref}$ (129/256)
10000000	$-V_{ref}$ (128 256) − V_{ref} 2
01111111	$-V_{ref}$ (127 256)
00000001	$-V_{ref}$ (1 256)
00000000	0

TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DIGITAL INPUT (SEE NOTE 6) MSB LSB	ANALOG OUTPUT
11111111	V_{ref} (127/128)
10000001	V_{ref} (1/128)
10000000	0
01111111	V_{ref} (1/128)
00000001	$-V_{ref}$ (127/128)
00000000	$-V_{ref}$

NOTES 5 LSB 1/256 (V_{ref})
6 LSB 1 128 (V_{ref})

microprocessor interfaces

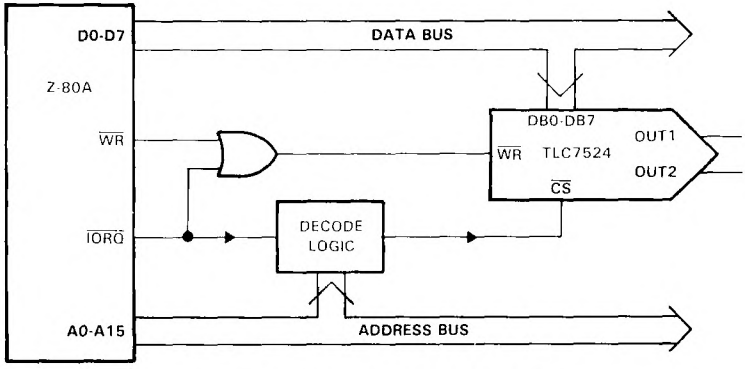

FIGURE 4. TLC7524–Z-80A INTERFACE

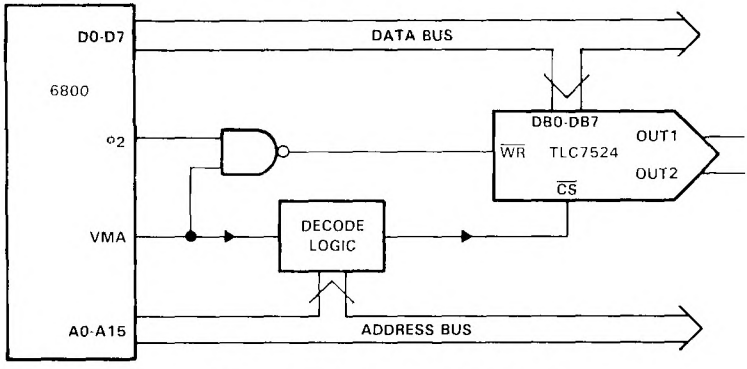

FIGURE 5. TLC7524–6800 INTERFACE

microprocessor interfaces (continued)

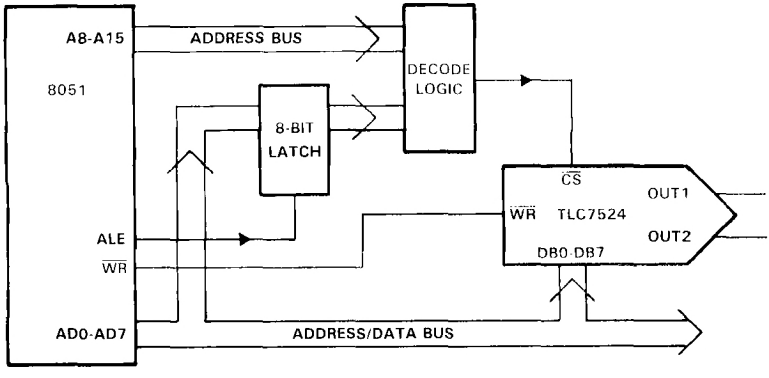

FIGURE 6. TLC7524—8051 INTERFACE

TYPICAL APPLICATION DATA

voltage-mode operation

It is possible to operate the TLC7524 current multiplying D/A converter in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output pin. The analog output voltage is then available at the reference voltage pin. Figure 7 is an example of a current multiplying D/A, which is operated in voltage mode.

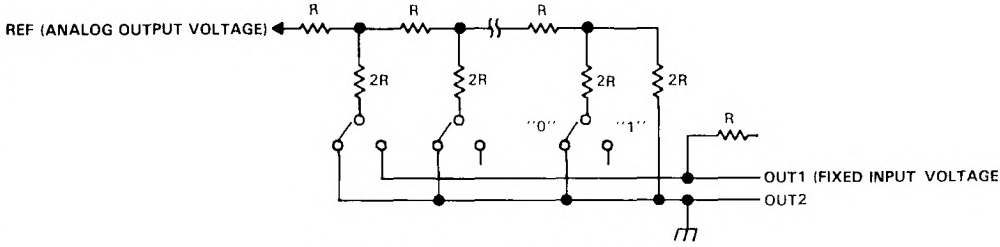

FIGURE 7. VOLTAGE MODE OPERATION

The relationship between the fixed input voltage and the analog output voltage is given by the following equation:

$$V_O = V_I (D/256)$$

where

V_O = analog output voltage
V_I = fixed input voltage
D = digital input code converted to decimal

In voltage-mode operation, the TLC7524 will meet the following specification:

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error at REF	V_{DD} = 5 V, OUT1 = 2.5 V, OUT2 at GND, T_A = 0°C to 70°C		1	LSB

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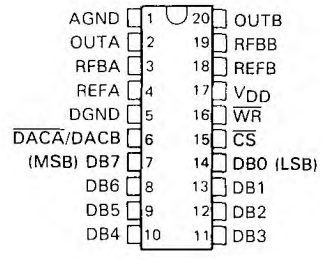
D2979, JANUARY 1987--REVISED OCTOBER 1988

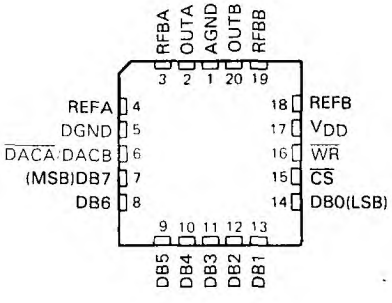
- Advanced LinCMOS™ Silicon-Gate Technology
- Easily Interfaced to Microprocessors
- On-Chip Data Latches
- Monotonic Over the Entire A/D Conversion Range
- Designed to be Interchangeable with Analog Devices AD7528 and PMI PM-7528
- Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320
- Voltage-Mode Operation

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 bits
Linearity Error	1/2 LSB
Power Dissipation at V_{DD} = 5 V	5 mW
Settling Time at V_{DD} = 5 V	100 ns
Propagation Delay at V_{DD} = 5 V	80 ns

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



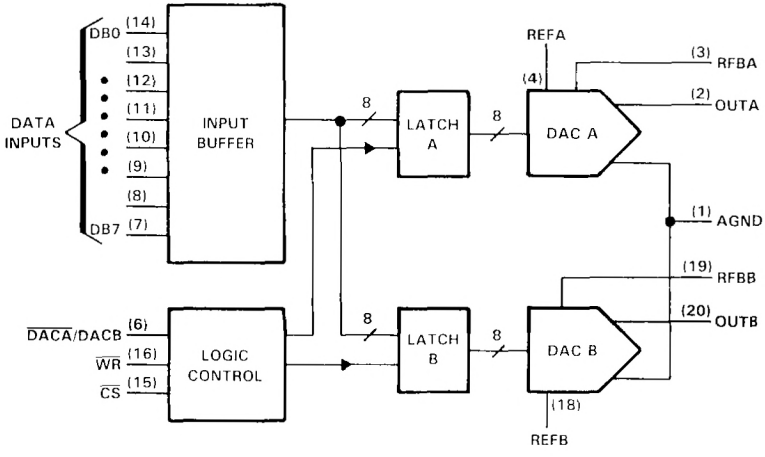
description

The TLC7528 is a dual 8-bit digital-to-analog converter designed with separate on-chip data latches and featuring excellent DAC-to-DAC matching. Data is transferred to either of the two DAC data latches via a common 8-bit input port. Control input $\overline{DACA}$/DACB determines which DAC is to be loaded. The "load" cycle of the TLC7528 is similar to the "write" cycle of a random-access memory, allowing easy interface to most popular microprocessor busses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

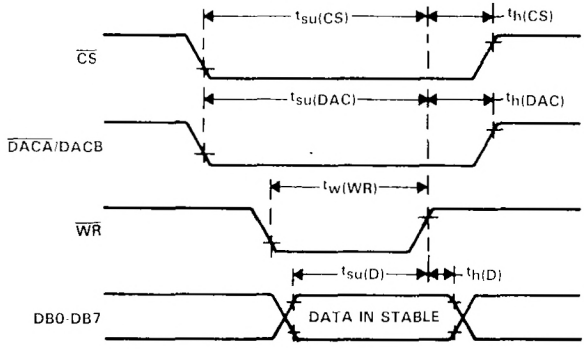
The TLC7528 operates from a 5-V to 15-V power supply and dissipates less than 15 mW (typical). Excellent 2- or 4-quadrant multiplying makes the TLC7528 a sound choice for many microprocessor-controlled gain-setting and signal-control applications. It can be operated in voltage mode, which produces a voltage output rather than a current output. Refer to the typical application data in this data sheet.

The TLC7528I is characterized for operation from −25 to 85°C. The TLC7528C is characterized for operation from 0°C to 70°C.

functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (to AGND or DGND) . . . . . −0.3 V to 16.5 V
Voltage between AGND and DGND . . . . . ±V_{DD}
Input voltage, V_I (to DGND) . . . . . −0.3 V to V_{DD} + 0.3
Reference voltage, V_{refA} or V_{refB} (to AGND) . . . . . ±25 V
Feedback voltage V_{RFBA} or V_{RFBB} (to AGND) . . . . . ±25 V
Output voltage, V_{OA} or V_{OB} (to AGND) . . . . . ±25 V
Peak input current . . . . . 10 μA
Operating free-air temperature range: TLC7528I . . . . . −25°C to 85°C
TLC7528C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

recommended operating conditions

		V_{DD} = 4.75 V to 5.25 V			V_{DD} = 14.5 V to 15.5 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Reference voltage, V_{refA} or V_{refB}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$		50			50			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			0			ns
DAC select setup time, $t_{su(DAC)}$		50			50			ns
DAC select hold time, $t_{h(DAC)}$		10			10			ns
Data bus input setup time $t_{su(D)}$		25			25			ns
Data bus input hold time $t_{h(D)}$		0			0			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		50			50			ns
Operating free-air temperature, T_A	TLC7528I	−25		85	−25		85	°C
	TLC7528C	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$			10			10	μA
I_{IL}	Low-level input current		V_I = 0 V			−10			−10	μA
	Reference input impedance (Pin 15 to GND)			5	12	20	5	12	20	kΩ
I_{lkg}	Output leakage current	OUTA	DACA data latch loaded with 00000000, V_{refA} = ±10 V			±400			±200	nA
		OUTB	DACB data latch loaded with 00000000, V_{refB} = ±10 V			±400			±200	
	Input resistance match (REFA to REFB)					±1%			±1%	
	DC supply sensitivity, Δ gain/Δ V_{DD}		ΔV_{DD} = ±10%			0.04			0.02	%/%
I_{DD}	Supply current (quiescent)		DB0-DB7 at V_{IH}min or V_{IL}max			1			1	mA
I_{DD}	Supply current (standby)		DB0-DB7 at 0 V or V_{DD}			0.5			0.5	mA
C_i	Input capacitance	DB0-DB7				10			10	pF
		$\overline{WR}$, $\overline{CS}$ $\overline{DACA}$/DACB				15			15	
C_o	Output capacitance, (OUTA, OUTB)		DAC data latches loaded with 00000000			50			50	pF
			DAC data latches loaded with 11111111			120			120	

†All typical values are at T_A = 25°C

operating characteristics over recommended operating free-air temperature range, V_{refA} = V_{refB} = 10 V, V_{OA} and V_{OB} at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error					±1/2			±1/2	LSB
Settling time (to 1/2 LSB)		See Note 1			100			100	ns
Gain error		See Note 2			2.5			2.5	LSB
AC feedthrough	REFA to OUTA	See Note 3			−65			−65	dB
	REFB to OUTB				−65			−65	
Temperature coefficient of gain		See Note 4			0.007			0.0035	%FSR/°C
Propagation delay (from digital input to 90% of final analog output current)		See Note 5			80			80	ns
Channel-to-channel isolation	REFA to OUTB	See Note 6		77			77		dB
	REFB to OUTA	See Note 7		77			77		
Digital-to-analog glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C		160			440		nVs
Digital crosstalk glitch impulse area		Measured for code transition from 00000000 to 11111111, T_A = 25°C		30			60		nVs
Harmonic distortion		V_I = 6 V rms, f = 1 kHz, T_A = 25°C		−85			−85		dB

NOTES: 1. OUTA, OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
2. Gain error is measured using an internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
3. V_{ref} = 20 V peak-to-peak, 100-kHz sine wave; DAC data latches loaded with 00000000.
4. Temperature coefficient of gain measured from 0°C to 25°C or from 25°C to 70°C.
5. V_{refA} = V_{refB} = 10 V; OUTA/OUTB load = 100 Ω, C_{ext} = 13 pF; $\overline{WR}$ and $\overline{CS}$ at 0 V; DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.
6. Both DAC latches loaded with 11111111; V_{refA} = 20 V peak-to-peak, 100-kHz sine wave; V_{refB} = 0; T_A = 25°C.
7. Both DAC latches loaded with 11111111; V_{refB} = 20 V peak-to-peak, 100-kHz sine wave; V_{refA} = 0; T_A = 25°C.

principles of operation

The TLC7528 contains two identical 8-bit multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground pin 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current (I_{lkg}) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C. C_O is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of C_O is 50 pF to 120 pF maximum. The equivalent output resistance r_O varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

Interfacing the TLC7528 to a microprocessor is accomplished via the data bus, $\overline{CS}$, $\overline{WR}$, and $\overline{DACA}$/DACB control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the TLC7528 analog output, specified by the $\overline{DACA}$/DACB control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs is latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The digital inputs of the TLC7528 provide TTL compatibility when operated from a supply voltage of 5 V. The TLC7528 may be operated with any supply voltage in the range from 5 V to 15 V, however, input logic levels are not TTL compatible above 5 V.

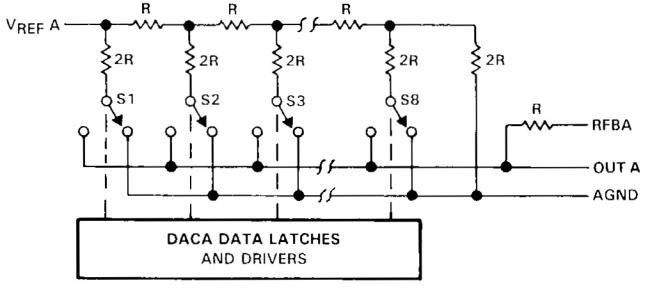


FIGURE 1. SIMPLIFIED FUNCTIONAL CIRCUIT FOR DACA

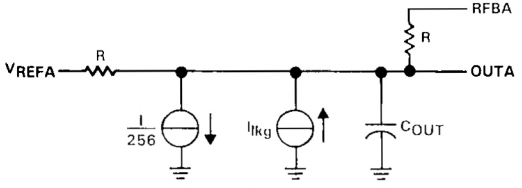


FIGURE 2. TLC7528 EQUIVALENT CIRCUIT, DACA LATCH LOADED WITH 11111111.

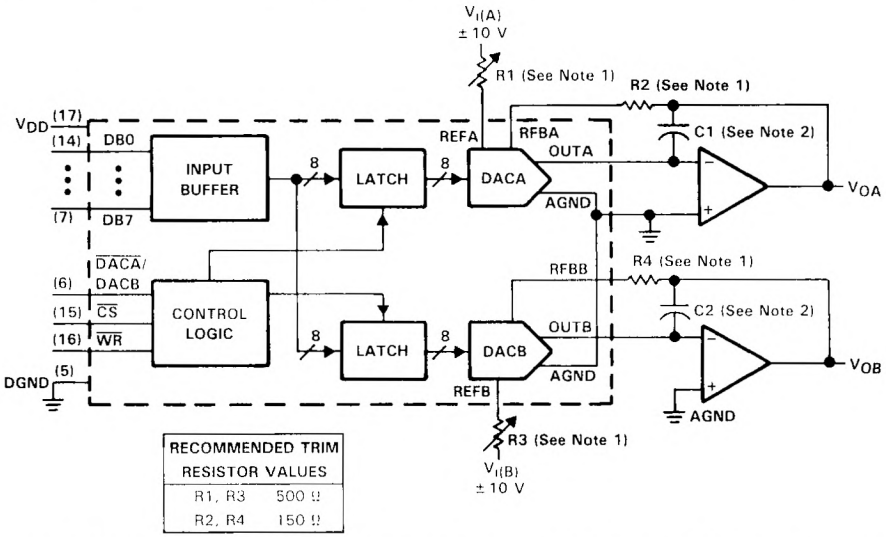
MODE SELECTION TABLE

$\overline{\text{DACA}}$/DACB	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = low level, H = high level, X = don't care

TYPICAL APPLICATION DATA

The TLC7528 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

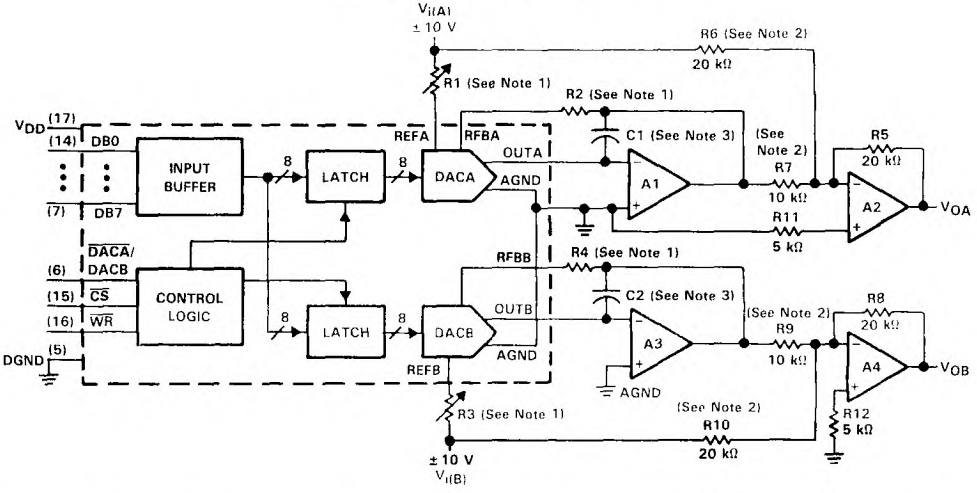


RECOMMENDED TRIM RESISTOR VALUES	
R1, R3	500 Ω
R2, R4	150 Ω

NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
2. C1 and C2 phase compensation capacitors (10 pF to 15 pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

FIGURE 3. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

TYPICAL APPLICATION DATA



NOTES: 1. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for V_{OA} = 0 V with code 10000000 in DACA latch. Adjust R3 for V_{OB} = 0 V with 10000000 in DACB latch.
2. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
3. C1 and C2 phase compensation capacitors (10 pF to 15 pF) may be required if A1 and A3 are high-speed amplifiers

FIGURE 4. BIPOLAR OPERATION (4-QUADRANT OPERATION)

TABLE 1. UNIPOLAR BINARY CODE

DAC LATCH CONTENTS MSB LSB†	ANALOG OUTPUT
11111111	$-V_i$ (255/256)
10000001	$-V_i$ (129/256)
10000000	$-V_i$ (128/256) = $-V_i/2$
01111111	$-V_i$ (127/256)
00000001	$-V_i$ (1/256)
00000000	$-V_i$ (0/256) = 0

† 1 LSB = $(2^{-8})V_i$

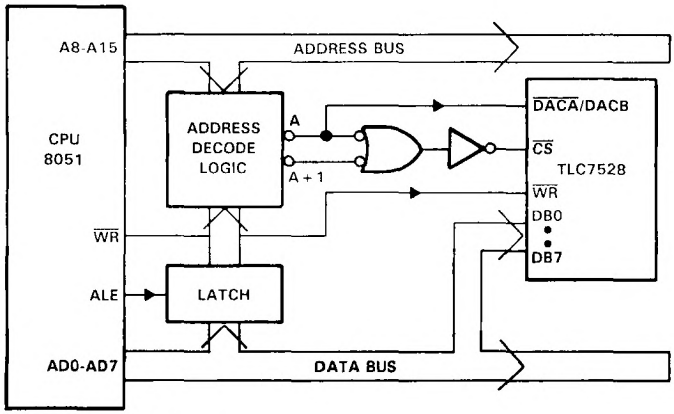
TABLE 2. BIPOLAR (OFFSET BINARY) CODE

DAC LATCH CONTENTS MSB LSB‡	ANALOG OUTPUT
11111111	V_i (127/128)
10000001	V_i (1/128)
10000000	0 V
01111111	$-V_i$ (1/128)
00000001	$-V_i$ (127/128)
00000000	$-V_i$ (128/128)

‡ 1 LSB = $(2^{-7})V_i$

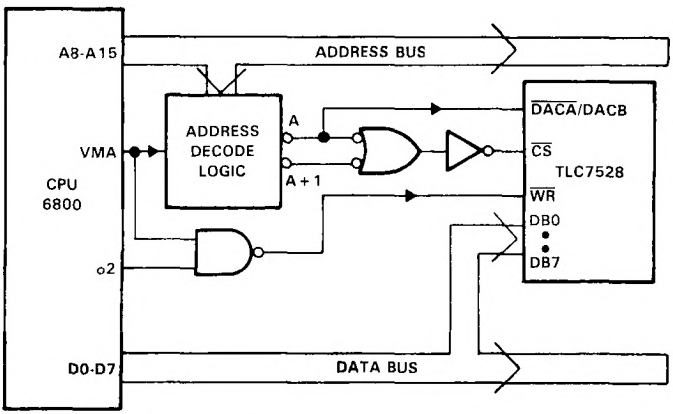
TYPICAL APPLICATION DATA

microprocessor interface information



NOTE: A = decoded address for TLC7528 DACA.
A + 1 = decoded address for TLC7528 DACB

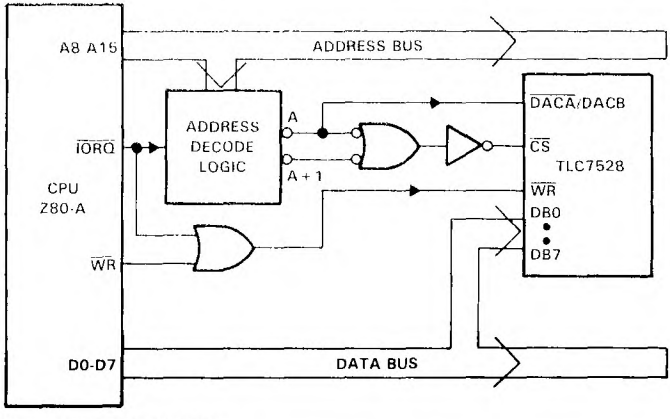
FIGURE 5. TLC7528 — INTEL 8051 INTERFACE



NOTE: A = decoded address for TLC7528 DACA.
A + 1 = decoded address for TLC7528 DACB.

FIGURE 6. TLC7528 — 6800 INTERFACE

TYPICAL APPLICATION DATA



NOTE: A = decoded address for TLC7528 DACA.
A + 1 = decoded address for TLC7528 DACB.

FIGURE 7. TLC7528 TO Z80-A INTERFACE

programmable window detector

The programmable window comparator shown in Figure 8 will determine if voltage applied to the DAC feedback resistors are within the limits programmed into the TLC7528 data latches. Input signal range depends on the reference and polarity, that is, the test input range is 0 to $-V_{ref}$. The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output high.

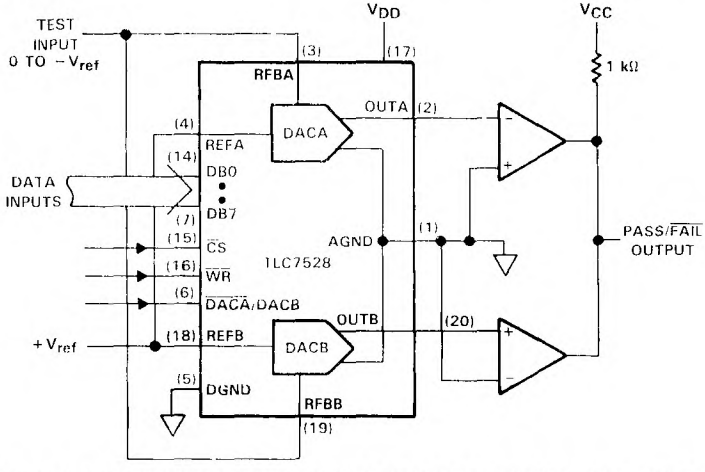


FIGURE 8. DIGITALLY PROGRAMMABLE WINDOW COMPARATOR (UPPER- AND LOWER-LIMIT TESTER)

TYPICAL APPLICATION DATA

digitally controlled signal attenuator

Figure 9 shows the TLC7528 configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5 dB range.

Attenuation dB = 20 log10 D/256, D = digital input code

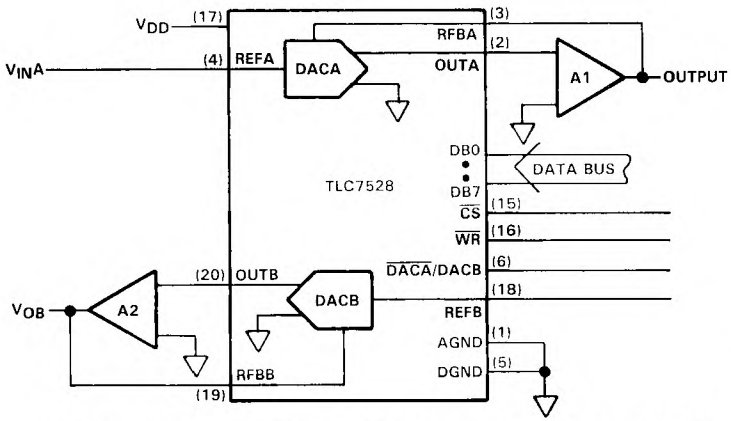


FIGURE 9. DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR

TABLE 3. ATTENUATION vs DACA, DACB CODE

ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL	ATTN(dB)	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10010000	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	1000(	128	14.0	00110011	51
6.5	0111	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43

TYPICAL APPLICATION DATA

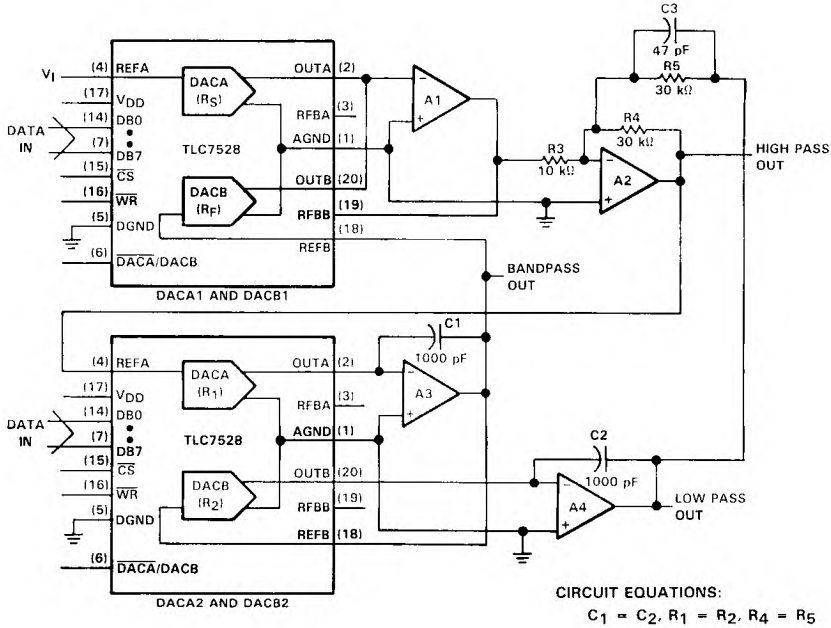
programmable state-variable filter

This programmable state-variable or universal filter configuration provides low-pass, high-pass, and band-pass outputs, and is suitable for applications in which microprocessor control of filter parameters is required.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the TLC7528, this is easily achieved.

$$f_C = \frac{1}{2\pi\, R1\, C1}$$

The programmable range for the cutoff or center frequency is 0 to 15 kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.



CIRCUIT EQUATIONS:

$$C_1 = C_2,\ R_1 = R_2,\ R_4 = R_5$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{fb(DACB1)}}$$

$$A_o = -\frac{R_F}{R_S}$$

NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.

B. C3 compensates for the op-amp gain-bandwidth limitations.

C. DAC equivalent resistance equals $\frac{256 \times (\text{DAC ladder resistance})}{\text{DAC digital code}}$

FIGURE 10. DIGITALLY CONTROLLED STATE-VARIABLE FILTER

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TYPICAL APPLICATION DATA

voltage-mode operation

It is possible to operate the TLC7528 current multiplying D/A converter in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output pin. The analog output voltage is then available at the reference voltage pin. Figure 11 is an example of a current multiplying D/A, which is operated in voltage mode.

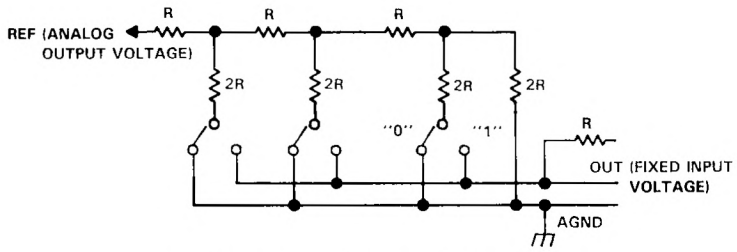


FIGURE 11. VOLTAGE-MODE OPERATION

The relationship between the fixed input voltage and the analog output voltage is given by the following equation:

$$V_O = V_I (D/256)$$

where

V_O = analog output voltage
V_I = fixed input voltage
D = digital input code converted to decimal

In voltage-mode operation, the TLC7528 will meet the following specification:

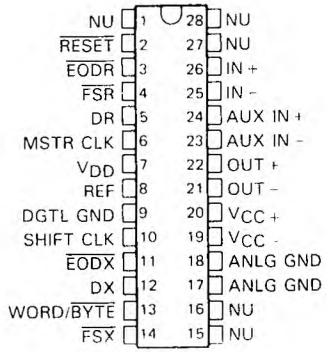
PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error at , or REFB	V_{DD} = 5 V, OUTA or OUTB at 2.5 V, T_A = 0°C to 70°C		1	LSB

D2964, SEPTEMBER 1987 – REVISED SEPTEMBER 1988

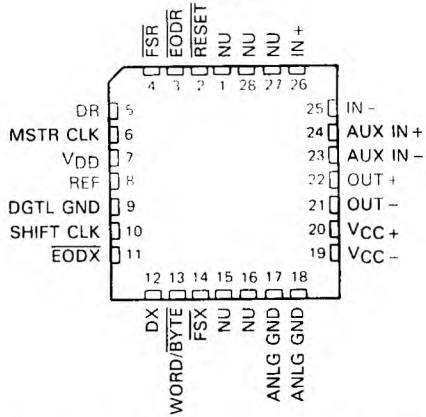
- Advanced LinCMOS™ Silicon-Gate Process Technology
- 14-Bit Dynamic Range ADC and DAC
- Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second
- Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter
- Serial Port for Direct Interface to TMS32011, TMS320C17, TMS32020, and TMS320C25 Digital Processors
- Synchronous or Asynchronous ADC and DAC Conversion Rates with Programmable Incremental ADC and DAC Conversion Timing Adjustments
- Serial Port Interface to SN74299 Serial-to-Parallel Shift Register for Parallel Interface to TMS32010, TMS320C15, or Other Digital Processors

PART NUMBER	DESCRIPTION
TLC32040	Analog Interface Circuit with internal reference. Also a plug-in replacement for TLC32041
TLC32041	Analog Interface Circuit without internal reference.
TLC32042	Identical to TLC32040, but has a slightly wider bandpass filter bandwidth

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NU – Nonusable, no external connection should be made to these pins

description

The TLC32040, TLC32041, and TLC32042 are complete analog-to-digital and digital-to-analog input/output systems, each on a single monolithic CMOS chip. This device integrates a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter. The device offers numerous combinations of Master Clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for this IC include modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), speech recognition/storage systems, industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS32011, TMS320C17, TMS32020, and TMS320C25 digital signal processors, are provided. Also, when the transmit and receive sections of the Analog Interface Circuit (AIC) are operating synchronously, it will interface to two SN74299

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description (continued)

serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the TMS32010, TMS320C15, other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of the IC can be selected and adjusted coincidentally with signal processing via software control.

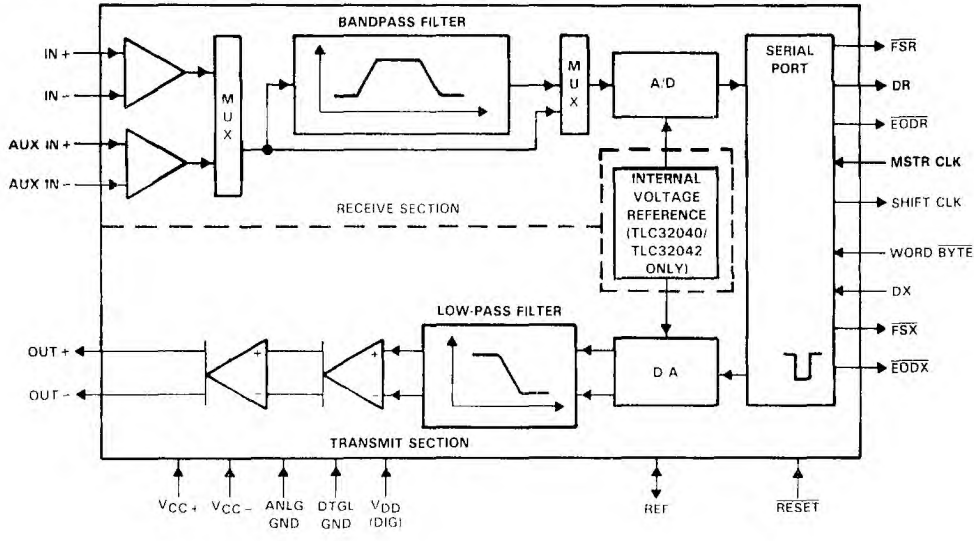
The antialiasing input filter comprises seventh-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively, and a fourth-order equalizer. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When no filtering is desired, the entire composite filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A converters each have 14 bits of resolution. The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided on the TLC32040 and TLC32042 to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to a pin and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is a seventh-order CC-type (Chebyshev/elliptic transitional low-pass filter with a fourth-order equalizer) and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal.

The TLC32040I, TLC32041I, and TLC32042I are characterized for operation from −40°C to 85°C, and the TLC32040C, TLC32041C, and TLC32042C are characterized for operation from 0°C to 70°C.

functional block diagram



analog input

Two sets of analog inputs are provided. Normally, the IN+ and IN− input set is used; however, the auxiliary input set, AUX IN+ and AUX IN−, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN+, IN−, AUX IN+, and AUX IN− inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D bandpass filter, A/D bandpass filter clocking, and A/D conversion timing

The A/D bandpass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz. The low-frequency roll-off of the high-pass section is 300 Hz. However, the high-pass section low-frequency roll-off is less steep for the TLC32042 than for the TLC32040 and TLC32041.

The Internal Timing Configuration and AIC DX Data Word Format sections of this data sheet indicate the many options for attaining a 288-kHz bandpass switched-capacitor filter clock. These sections indicate that the RX Counter A can be programmed to give a 288-kHz bandpass switched-capacitor filter clock for several Master Clock input frequencies.

The A/D conversion rate is then attained by frequency-dividing the 288-kHz bandpass switched-capacitor filter clock with the RX Counter B. Thus, unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the bandpass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample-and-hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output of the D/A low-pass filter to greatly attenuate any switched-capacitor clock feedthrough.

The D/A conversion rate is then attained by frequency-dividing the 288-kHz switched-capacitor filter clock with TX Counter B. Thus, unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

PRINCIPLES OF OPERATION (continued)

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (bandpass filter and ADC) are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the Master Clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and bandpass filters. In synchronous operation, the A/D conversion timing is derived from, and is equal to, the D/A conversion timing. (See description of the WORD/$\overline{\text{BYTE}}$ pin in the Pin Functional Description Section.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample-and-hold that is realized with a switched-capacitor ladder.

system frequency response correction

Sin x/x correction circuitry is performed in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 dB accuracy to a band-edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the sin x/x Correction Section for more details).

serial port

The serial port has four possible modes that are described in detail in the Functional Pin Description Section. These modes are briefly described below and in the Functional Description for Pin 13, WORD/$\overline{\text{BYTE}}$.

1. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32011 and TMS320C17.
2. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020 and the TMS320C25.
3. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32011 and TMS320C17.
4. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, or two SN74299 serial-to-parallel shift registers, which can then interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry.

testing

An addendum accompanying this data sheet fully describes the test capabilities of the IC, provided by the design.

operation of TLC32040 or TLC32042 with internal voltage reference

The internal reference of the TLC32040 and TLC32042 eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete control over the performance of the IC. The internal reference is brought out to a pin and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor may be connected between REF and ANLG GND.

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PRINCIPLES OF OPERATION (continued)

operation of TLC32040, TLC32041, or TLC32042 with external voltage reference

The REF pin may be driven from an external reference circuit if so desired. This external circuit must be capable of supplying 250 μA and must be adequately protected from noise such as crosstalk from the analog input.

reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset fun · · will initialize all AIC registers, including the control register. After a negative-going pulse on the ·· · $\overline{T}$ pin, the AIC will be initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section).

loopback

This feature allows the user to test the circuit remotely. In loopback, the OUT+ and OUT− pins are internally connected to the IN+ and IN− pins. Thus, the DAC bits (d15 to d2), which are transmitted to the DX pin, can be compared with the ADC bits (d15 to d2), which are received from the DR pin. An ideal comparison would be that the bits on the DR pin equal the bits on the DX pin. However, in practice there will be some difference in these bits due to the ADC and DAC output offsets.

In loopback, if the IN+ and IN− pins are enabled, the external signals on the IN+ and IN− pins are ignored. If the AUX IN+ and AUX IN− pins are enabled, the external signals on these pins are added to the OUT+ and OUT− signals in loopback operation.

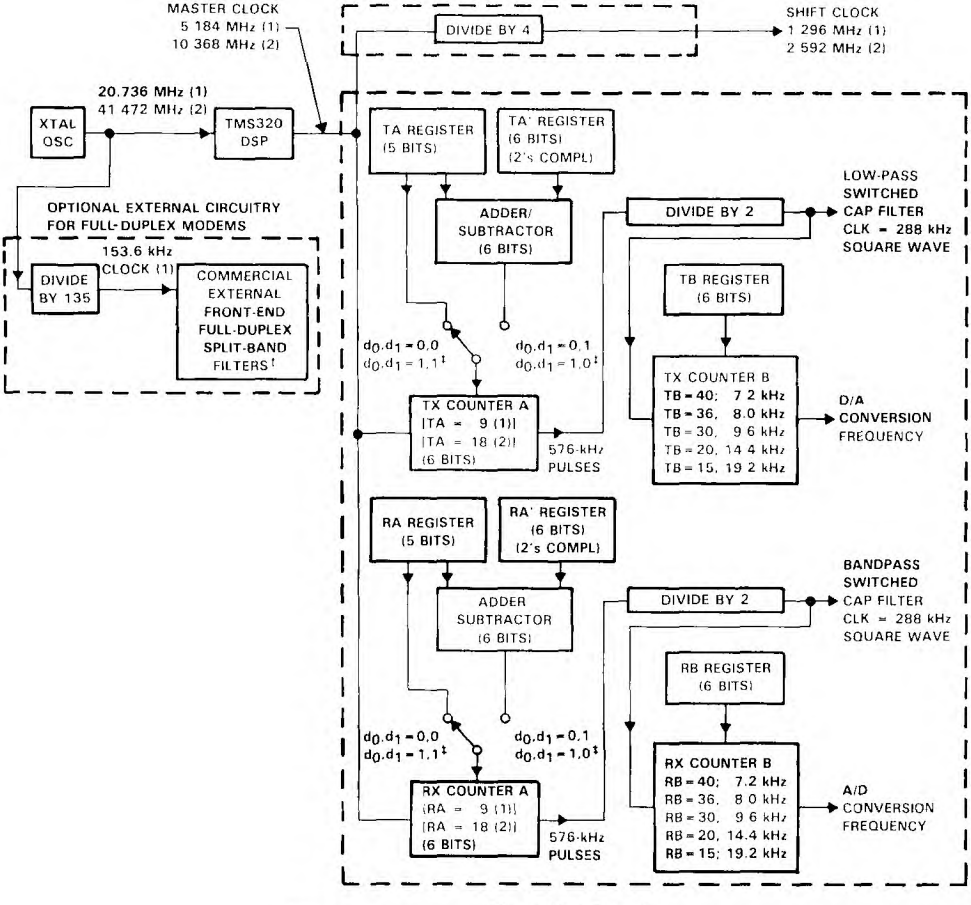
The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC Data Word Format section).

PIN NAME	PIN NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. This input can be switched into the bandpass filter and A/D converter path via software control. If the appropriate bit in the Control register is a 1, the auxiliary inputs will replace the IN+ and IN− inputs. If the bit is a 0, the IN+ and IN− inputs will be used (see the AIC DX Data Word Format section).
AUX IN−	23	I	Inverting auxiliary analog input (see the above AUX IN+ pin description).
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	This pin is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	This pin is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port to the AIC is synchronized with the SHIFT CLK signal.
$\overline{\text{EODR}}$	3	O	(See the WORD/$\overline{\text{BYTE}}$ pin description and the Serial Port Timing Diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS32011 or TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.

PIN NAME	PIN NO.	I/O	DESCRIPTION
	11	O	(See the WORD/$\overline{\text{BYTE}}$ pin description and the Serial Port Timing Diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the TMS320 serial port to the AIC. This signal can be used to interrupt a microprocessor upon the completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS32011 or TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
$\overline{\text{FSR}}$	4	O	In the serial transmission modes, which are described in the WORD/$\overline{\text{BYTE}}$ pin description, the $\overline{\text{FSR}}$ pin is held low during bit transmission. When the $\overline{\text{FSR}}$ pin goes low, the TMS320 serial port will begin receiving bits from the AIC via the DR pin of the AIC. The most significant DR bit will be present on the DR pin before $\overline{\text{FSR}}$ goes low. (See Serial Port Timing and Internal Timing Configuration Diagrams.)
$\overline{\text{FSX}}$	14	O	When this pin goes low, the TMS320 serial port will begin transmitting bits to the AIC via the DX pin of the AIC. In all serial transmission modes, which are described in the WORD/$\overline{\text{BYTE}}$ pin description, the $\overline{\text{FSX}}$ pin is held low during bit transmission (see Serial Port Timing and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN−	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The Master Clock signal is used to derive all the key logic signals of the AIC, such as the Shift Clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the Master Clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT−	21	O	Inverting output of analog output power amplifier. Functionally identical with and complementary to OUT+.
REF	8	I/O	For the TLC32040 and TLC32042, the internal voltage reference is brought out on this pin. For the TLC32040, TLC32041, and TLC32042, an external voltage reference can be applied to this pin.
	2	I	A reset function is provided to initialize the TA, TA′, TB, RA, RA′, RB, and control registers. This reset function initiates serial communications between the AIC and DSP. The reset function will initialize all AIC registers including the control register. After a negative-going pulse on the $\overline{\text{RESET}}$ pin, the AIC registers will be initialized to provide an 8-kHz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA′ and RA′, will be reset to 1. The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section). d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1 This initialization allows normal serial-port communication to occur between AIC and DSP.
SHIFT CLK	10	O	The Shift Clock signal is obtained by dividing the Master Clock signal frequency by four. This signal is used to clock the serial data transfers of the AIC, described in the WORD/$\overline{\text{BYTE}}$ pin description below (see the Serial Port Timing and Internal Timing Configuration diagram).
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage −5 V ±5%

PIN NAME	NO.	I/O	DESCRIPTION
WORD/$\overline{\text{BYTE}}$	13	I	This pin, in conjunction with a bit in the CONTROL register, is used to establish one of four serial modes. These four serial modes are described below. *AIC transmit and receive sections are operated asynchronously.* The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the Control register is a 0 (see the AIC DX Data Word Format), the transmit and receive sections will be asynchronous. L Serial port directly interfaces with the serial port of the TMS32011 or TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams). 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought low. 4. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin emits a positive frame-sync pulse that is four Shift Clock cycles wide. 5. One 8-bit byte is transmitted or one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought high. 7. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. H Serial port directly interfaces with the serial port of the TMS32020, TMS320C25, or TMS320C30 and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 16-bit word is transmitted or one 16-bit word is received. 3. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin emits a low-going pulse. *AIC transmit and receive sections are operated synchronously.* If the appropriate data bit in the Control register is a 1, the transmit and receive sections will be configured to be synchronous. In this case, the bandpass switched-capacitor filter and the A/D conversion timing will be derived from the TX Counter A, TX Counter B, and TA, TA', and TB registers, rather than the RX Counter A, RX Counter B, and RA, RA', and RB registers. In this case, the AIC $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ timing will be identical during primary data communication; however, $\overline{\text{FSR}}$ will not be asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Serial Port Timing diagrams). L Serial port directly interfaces with the serial port of the TMS32011 or TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought low. 4. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins emit positive frame-sync pulses that are four Shift Clock cycles wide. 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought high. 7. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. H Serial port directly interfaces with the serial port of the TMS32020, TMS320C25, or TMS320C30 and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 16-bit word is transmitted and one 16-bit word is received. 3. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pins emit low-going pulses. Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port, with additional NOR and AND gates, will interface to two SN74299 serial-to-parallel shift registers. Interfacing the AIC to the SN74299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel, data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Serial Port Timing diagrams).

INTERNAL TIMING CONFIGURATION



$$\text{SCF Clock Frequency} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

NOTE: Frequency 1, 20.736 MHz, is used to show how 153.6 kHz (for a commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2, 41.472 MHz, is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.

†Split-band filtering can alternatively be performed after the analog input function via software in the TMS320.

‡These control bits are described in the AIC DX Data Word Format section.

explanation of internal timing configuration

All of the internal timing of the AIC is derived from the high-frequency clock signal that drives the Master Clock input pin. The Shift Clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the Master Clock input signal frequency by four.

$$\text{SCF Clock Frequency} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency}}{\text{Contents of Counter B}}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master Clock Frequency}}{4}$$

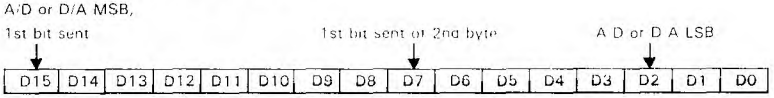
TX Counter A and TX Counter B, which are driven by the Master Clock signal, determine the D/A conversion timing. Similarly, RX Counter A and RX Counter B determine the A/D conversion timing. In order for the switched-capacitor low-pass and bandpass filters to meet their transfer function specifications, the frequency of the clock inputs of the switched-capacitor filters must be 288 kHz. If the frequencies of the clock inputs are not 288 kHz, the filter transfer function frequencies are scaled by the ratios of the clock frequencies to 288 kHz. Thus, to obtain the specified filter responses, the combination of Master Clock frequency and TX Counter A and RX Counter A values must yield 288-kHz switched-capacitor clock signals. These 288-kHz clock signals can then be divided by the TX Counter B and RX Counter B to establish the D/A and A/D conversion timings.

TX Counter A and TX Counter B are reloaded every D/A conversion period, while RX Counter A and RX Counter B are reloaded every A/D conversion period. The TX Counter B and RX Counter B are loaded with the values in the TB and RB Registers, respectively. Via software control, the TX Counter A can be loaded with either the TA Register, the TA Register less the TA' Register, or the TA Register plus the TA' Register. By selecting the TA Register less the TA' Register option, the upcoming conversion timing will occur earlier by an amount of time that equals TA' times the signal period of the Master Clock. By selecting the TA Register plus the TA' Register option, the upcoming conversion timing will occur later by an amount of time that equals TA' times the signal period of the Master Clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX Counter A can be programmed via software control with the RA Register, the RA Register less the RA' Register, or the RA Register plus the RA' Register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous (see WORD/$\overline{\text{BYTE}}$ pin description), then both the low-pass and bandpass switched-capacitor filter clocks are derived from TX Counter A. Also, both the D/A and A/D conversion timing are derived from the TX Counter A and TX Counter B. When the transmit and receive sections are configured to be synchronous, the RX Counter A, RX Counter B, RA Register, RA' Register, and RB Registers are not used.

AIC DR or DX word bit pattern



AIC DX data word format section

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d2	d1	d0	COMMENTS
primary DX serial communication protocol															
← d15 (MSB) through d2 go to the D/A converter register →													0	0	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with TB and RB register values.
← d15 (MSB) through d2 go to the D/A converter register →													0	1	The TX and RX Counter A's are loaded with the TA + TA' and RA + RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 0, d0 = 1 will cause the next D/A and A/D conversion periods to be changed by the addition of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →													1	0	The TX and RX Counter A's are loaded with the TA − TA' and RA − RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 1, d0 = 0 will cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →													1	1	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with the TB and RB register values. After a delay of four Shift Clock cycles, a secondary transmission will immediately follow to program the AIC to operate in the desired configuration.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (Primary Communications) to the AIC will initiate Secondary Communications upon completion of the Primary Communications.

Upon completion of the Primary Communication, $\overline{FSX}$ will remain high for four SHIFT CLOCK cycles and will then go low and initiate the Secondary Communication. The timing specifications for the Primary and Secondary Communications are identical. In this manner, the Secondary Communication, if initiated, is interleaved between successive Primary Communications. This interleaving prevents the Secondary Communication from interfering with the Primary Communications and DAC timing, thus preventing the AIC from skipping a DAC output. It is important to note that in the synchronous mode, $\overline{FSR}$ will not be asserted during Secondary Communications.

secondary DX serial communication protocol

x x ← to TA register → x x ← to RA register → 0 0	d13 and d6 are MSBs (unsigned binary)
x ← to TA′ register → x ← to RA′ register → 0 1	d14 and d7 are 2's complement sign bits
x ← to TB register → x ← to RB register → 1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x x x d7 d6 d5 d4 d3 d2 1 1 ← CONTROL REGISTER →	d2 = 0/1 deletes inserts the bandpass filter d3 = 0/1 disables/enables the loopback function d4 = 0/1 disables/enables the AUX IN + and AUX IN − pins d5 = 0/1 asynchronous/synchronous transmit and receive sections d6 = 0/1 gain control bits (see Gain Control Section) d7 = 0/1 gain control bits (see Gain Control Section)

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function will initialize all AIC registers, .ing the control register. After power has been applied to the AIC, a negative-going pulse on the · · · pin will initialize the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184 MHz master clock input signal. The AIC, excepting the CONTROL register, will be initialized as follows (see AIC DX Data Word Format section):

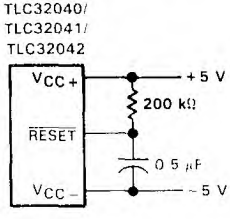
REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA′	1
TB	24
RA	9
RA′	1
RB	24

The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section):

d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA′, and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the Pin Descriptions and AIC DX Word Format sections).

The circuit shown below will provide a reset on power-up when power is applied in the sequence given under Power-Up Sequence. The circuit depends on the power supplies' reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.



power-up sequence

To ensure proper operation of the AIC, and as a safeguard against latch-up, it is recommmended that a Schottky diode with a forward voltage less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND (see Figure 17). In the absence of such a diode, power should be applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal should be applied until after power-up.

AIC responses to improper conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 1 below.

AIC register constraints

The following constraints are placed on the contents of the AIC registers:

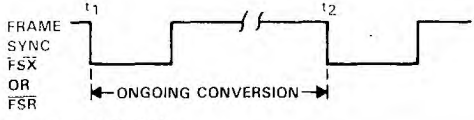
1. TA register must be > 1.
2. TA' register can be either positive, negative, or zero.
3. RA register must be > 1.
4. RA' register can be either positive, negative, or zero.
5. (TA register ± TA' register) must be > 1.
6. (RA register ± RA' register) must be > 1.
7. TB register must be > 1.

TABLE 1. AIC RESPONSES TO IMPROPER CONDITIONS

IMPROPER CONDITION	AIC RESPONSE
TA register + TA' register = 0 or 1 TA register − TA' register = 0 or 1	Reprogram TX Counter A with TA register value
TA register + TA' register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into the TX Counter A, i.e., TA register + TA' register + 40 HEX is loaded into TX Counter A
RA register + RA' register = 0 or 1 RA register − RA' register = 0 or 1	Reprogram RX Counter A with RA register value
RA register + RA' register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX Counter A, i.e., RA register + RA' register + 40 HEX is loaded into RX Counter A
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down
TB register = 0 or 1	Reprogram TB register with 24 HEX
RB register = 0 or 1	Reprogram RB register with 24 HEX
AIC and DSP cannot communicate	Hold last DAC output

improper operation due to conversion times being too close together

If the difference between two successive D/A conversion frame syncs is less that 1/19.2 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A' register or A − A' register result is too small. When incrementally adjusting the conversion period via the A + A' register options, the designer should be very careful not to violate this requirement (see diagram below).



$t_2 - t_1 < 1/19.2$ kHz

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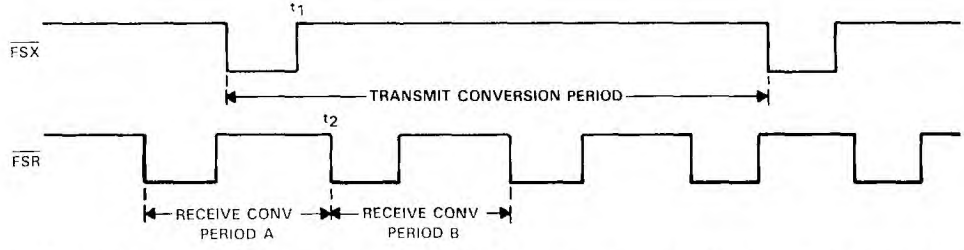
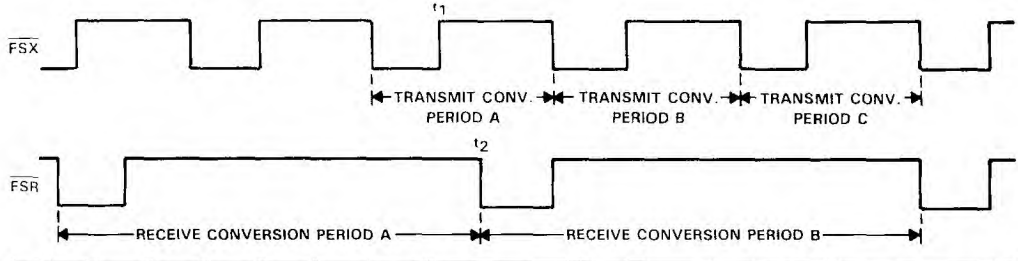
asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing conversion period is then adjusted. However, either Receive Conversion Period A or B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t1 and t2, the receive conversion period adjustment will be performed during Receive Conversion Period A. Otherwise, the adjustment will be performed during Receive Conversion Period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see figure below).



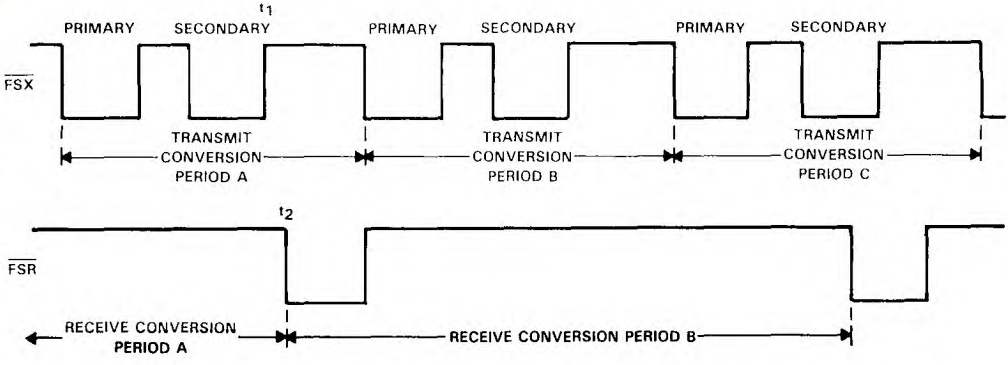
asynchronous operation — more than one transmit frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the figure below. If the adjustment command is issued during Transmit Conversion Period A, Receive Conversion Period A will be adjusted if there is sufficient time between t1 and t2. Or, if there is not sufficient time between t1 and t2, Receive Conversion Period B will be adjusted. Or, the receive portion of an adjustment command may be ignored if the adjustment command is sent during a receive conversion period, which is already being or will be adjusted due to a prior adjustment command. For example, if adjustment commands are issued during Transmit Conversion Periods A, B, and C, the first two commands may cause Receive Conversion Periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during Receive Conversion Period B, which already will be adjusted via the Transmit Conversion Period B adjustment command.



asynchronous operation — more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX Data Word Format section)

The TA, TA', TB, and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t1 and t2, the TA, RA', and RB register information, which is sent during Transmit Conversion Period A, will be applied to Receive Conversion Period A. Otherwise, this information will be applied during Receive Conversion Period B. If RA, RA', and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA, RA', or RB information that is received during this receive conversion period will be disregarded (see diagram below).



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	−0.3 V to 15 V
Supply voltage, V_{DD}	**−0.3 V to 15 V**
Output voltage, V_O	**−0.3 V to 15 V**
Input voltage, V_I	−0.3 V to 15 V
Digital ground voltage	−0.3 V to 15 V
Operating free-air temperature range: TLC32040I, TLC32041I, TLC32042I	−40°C to 85°C
TLC32040C, TLC32041C, TLC32042C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

NOTE 1: Voltage values for maximum ratings are with respect to VCC−.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 3)		−0.3		0.8	V
Load resistance at OUT+ and/or OUT−, R_L		300			Ω
Load capacitance at OUT+ and/or OUT−, C_L				100	pF
MSTR CLK frequency (see Note 4)		0.075	5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				19.2	kHz
Conversion rate		1		20	kHz
Operating free-air temperature, T_A	TLC32040I, TLC32041I, TLC32042I	−40		85	°C
	TLC32040C, TLC32041C, TLC32042C	0		70	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-}, are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.
4. The bandpass and low-pass switched-capacitor filter response specifications apply only when the switched-capacitor clock frequency is 288 kHz. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.
5. This range applies when (IN+ − IN−) or (AUX IN+ − AUX IN−) equals ±6 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TI[illegible]—C				35	mA
		TI[illegible]—I				40	
I_{CC-}	Supply current from V_{CC-}	TLC3204—C				−35	mA
		TLC3204—I				−40	
I_{DD}	Supply current from V_{DD}		$f_{MSTR\ CLK}$ = 5.184 MHz			7	mA
V_{ref}	Internal reference output voltage			3		3.3	V
αV_{ref}	Temperature coefficient of internal reference voltage				100		ppm/°C
r_o	Output resistance at REF				100		kΩ

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters bypassed)			25	65	mV
	A/D converter offset error (filters in)			25	65	mV
CMRR	Common-mode rejection ratio at IN+, IN−, or AUX IN+, AUX IN−	See Note 6		55		dB
r_i	Input resistance at IN+, IN− or AUX IN+, AUX IN−, REF			100		kΩ

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT− (single-ended relative to ANLG GND)			15	75	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT− (single-ended)	R_L = 300 Ω, Offset voltage = 0	±3			V
V_{OM}	Maximum peak output voltage swing between OUT+ and OUT− (differential output)	$R_L \geq$ 600 Ω	±6			V

†All typical values are at T_A = 25°C.

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with an 8-kHz conversion rate.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

system distortion specifications, SCF clock frequency = 288 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	V_{in} = −0.1 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended	V_{in} = −0.1 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	differential		57	65		
Attenuation of second harmonic of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	differential		57	65		

A/D channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	A_v = 1‡		A_v = 2‡		A_v = 4‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	58		>58§		>58§		dB
	V_{in} = −12 dB to −6 dB	58		58		>58§		
	V_{in} = −18 dB to −12 dB	56		58		58		
	V_{in} = −24 dB to −18 dB	50		56		58		
	V_{in} = −30 dB to −24 dB	44		50		56		
	V_{in} = −36 dB to −30 dB	38		44		50		
	V_{in} = −42 dB to −36 dB	32		38		44		
	V_{in} = −48 dB to −42 dB	26		32		38		
	V_{in} = −54 dB to −48 dB	20		26		32		

D/A channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	58		dB
	V_{in} = −12 dB to −6 dB	58		
	V_{in} = −18 dB to −12 dB	56		
	V_{in} = −24 dB to −18 dB	50		
	V_{in} = −30 dB to −24 dB	44		
	V_{in} = −36 dB to −30 dB	38		
	V_{in} = −42 dB to −36 dB	32		
	V_{in} = −48 dB to −42 dB	26		
	V_{in} = −54 dB to −48 dB	20		

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Absolute transmit gain tracking error while transmitting into 600 Ω	−48 dB to 0 dB signal range, See Note 8		±0.05	±0.15	dB
Absolute receive gain tracking error	−48 dB to 0 dB signal range, See Note 8		±0.05	±0.15	dB

†All typical values are at T_A = 25°C
‡A_v is the programmable gain of the input amplifier.
§A value > 58 is overrange and signal clipping occurs.
NOTES: 7. The test condition is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω.
8 Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 db relative to V_{ref}).

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single-ended)				80		dB

delay distortion, SCF clock frequency = 288 kHz ±2%, input (IN+ − IN−) is ±3-V sinewave

Please refer to filter response graphs for delay distortion specifications.

TLC32040 and TLC32041 bandpass filter transfer function (see curves), SCF clock frequency = 288 kHz ±2%, input (IN+ − IN−) is a ±3-V sinewave (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Filter Gain (see Note 10)	Input signal reference is 0 dB	f = 100 Hz		−42	dB
		f = 170 Hz		−25	
		300 Hz ≤ f ≤ 3.4 kHz	−0.5	0.5	
		f = 4 kHz		−16	
		f ≥ 4.6 kHz		−58	

TLC32042 bandpass filter transfer function (see curves), SCF clock frequency = 288 kHz ±2%, input (IN+ − IN−) is a ±3-V sinewave (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Filter Gain (see Note 10)	Input signal reference is 0 dB	f = 100 Hz		−27	dB
		f = 170 Hz		−2	
		300 Hz ≤ f ≤ 3.4 kHz	−0.5	0.5	
		f = 4 kHz		−16	
		f ≥ 4.6 kHz		−58	

low-pass filter transfer function, SCF clock frequency = 288 kHz ±2% (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Filter Gain (see Note 10)	Output signal reference is 0 dB	f ≤ 3.4 kHz	−0.5	0.5	dB
		f = 3.6 kHz		−4	
		f = 4 kHz		−30	
		f ≥ 4.4 kHz		−58	

serial port

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −[illegible] µA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	µA
C_I	Input capacitance			15		pF
C_O	Output capacitance			15		pF

† All typical values are at T_A = 25°C.

NOTES: 9. The above filter specifications are for a switched-capacitor filter clock range of 288 kHz ±2%. For switched-capacitor filter clocks at frequencies other than 288 kHz ±2%, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

10. The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 300 to 3400 Hz and 0 to 3400 Hz for the bandpass and lowpass filters respectively.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

noise (measurement includes low-pass and bandpass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
Transmit noise	single-ended	DX input = 00000000000000, constant input code	200		μV rms
	differential		300	500	μV rms
			20		dBrnc0
Receive noise (see Note 11)		Inputs grounded, gain = 1	300	475	μV rms
			20		dBrnc0

timing requirements

serial port recommended input signals

PARAMETER			MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time		95		ns
$t_{r(MCLK)}$	Master clock rise time			10	ns
$t_{f(MCLK)}$	Master clock fall time			10	ns
	Master clock duty cycle		42%	58%	
	$\overline{RESET}$ pulse duration	Note 12)	800		ns
$t_{su(DX)}$	DX setup time before ↓		20		ns
$t_{h(DX)}$	DX hold time after SCLK↓		$t_{c(SCLK)}/4$		ns

† All typical values are at T_A = 25°C.

NOTES: 11. This noise is referred to the input with a buffer gain of one. If the buffer gain is two or four, the noise figure will be correspondingly reduced. The noise is computed by statistically evaluating the digital output of the A/D converter.

12 $\overline{RESET}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values

correction results

Table 4 below shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates.

TABLE 4

f (Hz)	ERROR (dB) f_S = 8000 Hz p1 = −0.14813 p2 = 0.9888	ERROR (dB) f_S = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	0.099	0.043
600	0.089	0.043
900	0.054	0
1200	0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	0.043	0
3000	−0.102	−0.043

TMS320 software requirements

The digital correction filter equation can be written in state variable form as follows:

$$Y = k1Y + k2U$$

where k1 equals p1 (from the preceding page), k2 equals (1 − p1)p2 (from the preceding page), Y is the filter state, and U is the next I/O sample. The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) will yield the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

sin x/x correction section

The AIC does not have sin x/x correction circuitry after the digital-to-analog converter. Sin x/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown below, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the TMS320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction will add a slight amount of group delay at the upper edge of the 300−3000-Hz band.

sin x/x roll-off for a zero-order hold function

The sin x/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

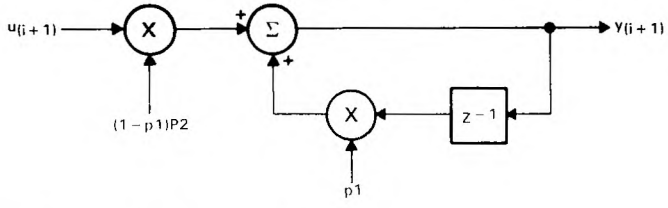
TABLE 3. sin x/x ROLL-OFF

f_S (Hz)	$20 \log \frac{\sin \pi f/f_S}{\pi f/f_S}$ (f = 3000 Hz) (dB)
7200	2 64
8000	- 2 11
9600	1 44
14400	- 0 63
19200	0 35

Note that the actual AIC sin x/x roll-off will be slightly less than the above figures, because the AIC has less than a 100-% duty cycle hold interval.

correction filter

To compensate for the sin x/x roll-off of the AIC, a first-order correction filter shown below, is recommended.



The difference equation for this correction filter is:

$$y_{i+1} = p2(1-p1)\,(u_{i+1}) + p1\,y_i$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{p2^2\,(1-p1)^2}{1 - 2p1\cos(2\pi f/f_S) + p1^2}$$

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (continued)

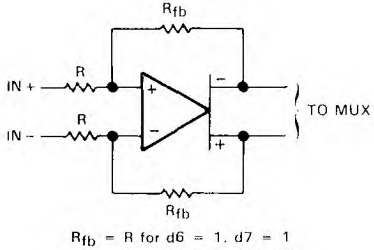
serial port — AIC output signals

	PARAMETER	MIN	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		50	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		50	ns
	Shift clock (SCLK) duty cycle	45	55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR/FSX}$↓		90	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR/FSX}$↑		90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑		90	ns
$t_{dw(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX/EODR}$↓ in word mode		90	ns
$t_{dw(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX/EODR}$↑ in word mode		90	ns
$t_{f(EODX)}$	$\overline{EODX}$ fall time		15	ns
$t_{f(EODR)}$	$\overline{EODR}$ fall time		15	ns
$t_{db(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX/EODR}$↓ in byte mode		100	ns
$t_{db(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX/EODR}$↑ in byte mode		100	ns

TABLE 2. GAIN CONTROL TABLE (ANALOG INPUT SIGNAL REQUIRED FOR FULL-SCALE A/D CONVERSION)

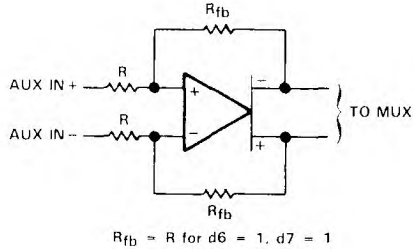
INPUT CONFIGURATIONS	CONTROL REGISTER BITS d6	CONTROL REGISTER BITS d7	ANALOG INPUT†	A/D CONVERSION RESULT
Differential configuration	1	1	±6 V	full-scale
Analog input = IN+ − IN−	0	0		
= AUX IN+ − AUX IN−	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale
Single-ended configuration	1	1	±3 V	half-scale
Analog input = IN+ − ANLG GND	0	0		
= AUX IN+ − ANLG GND	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale

† In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 1. IN+ AND IN− GAIN CONTROL CIRCUITRY

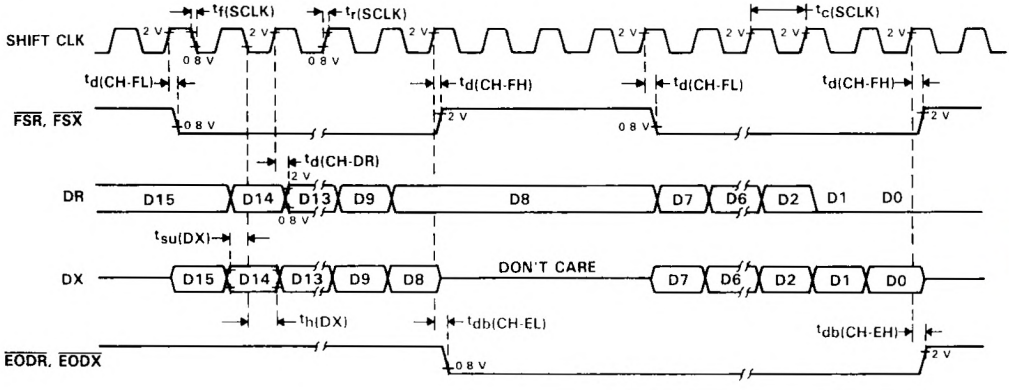


R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 2. AUX IN+ AND AUX IN− GAIN CONTROL CIRCUITRY

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

byte-mode timing



word-mode timing

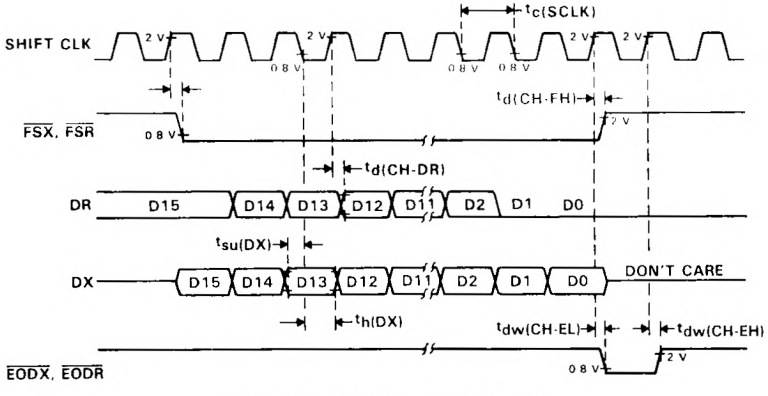


FIGURE 3. SERIAL PORT TIMING

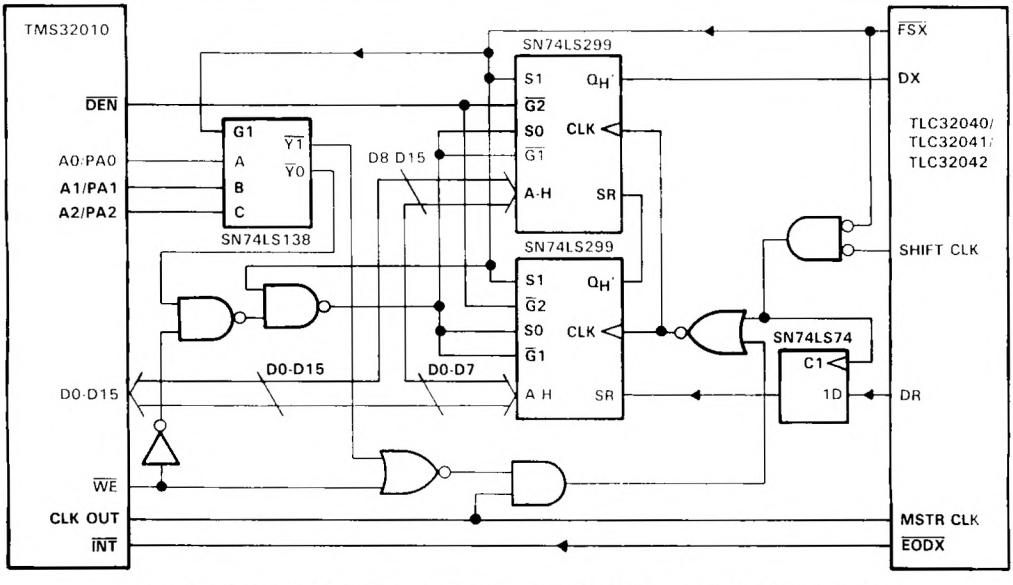
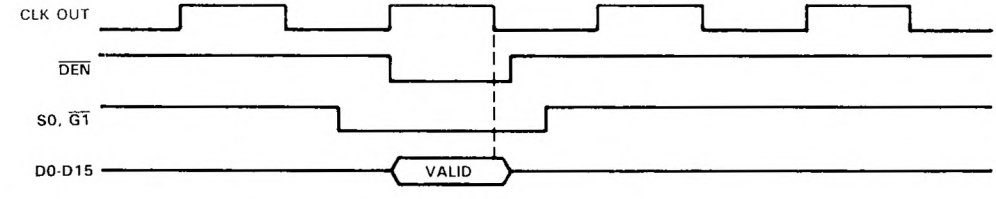


FIGURE 4. TMS32010-TLC32040/TLC32041/TLC32042 INTERFACE CIRCUIT

in instruction timing



out instruction timing

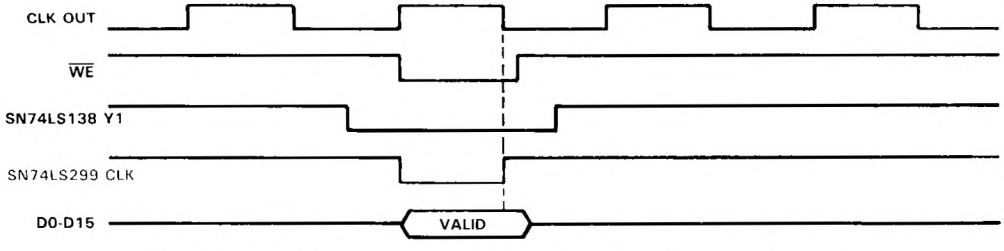
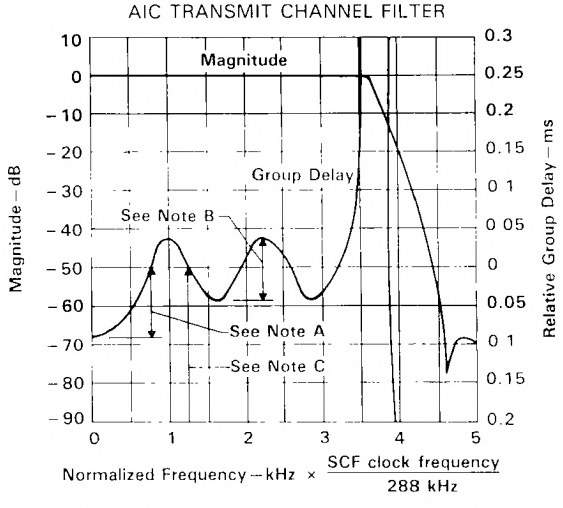


FIGURE 5. TMS32010-TLC32040/TLC32041/TLC32042 INTERFACE TIMING

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

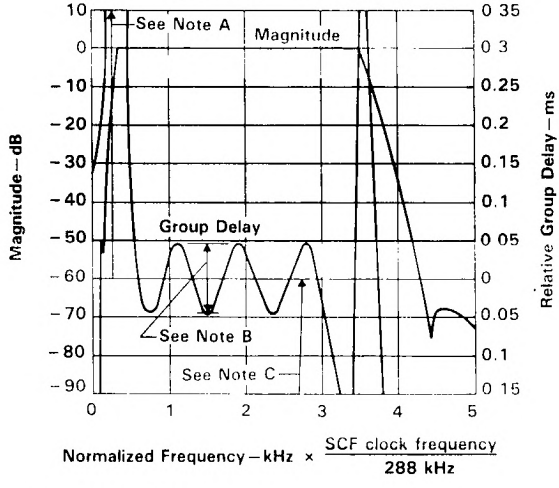


NOTES: A. Maximum relative delay (0 Hz to 600 Hz) = 125 μs.
B. Maximum relative delay (600 Hz to 3000 Hz) = ±50 μs.
C. Absolute delay (600 Hz to 3000 Hz) = 700 μs.
D. Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions, SCF clock f = 288 kHz ±2%, input = ±3-V sinewave, and T_A = 25°C.

FIGURE 6

TYPICAL CHARACTERISTICS

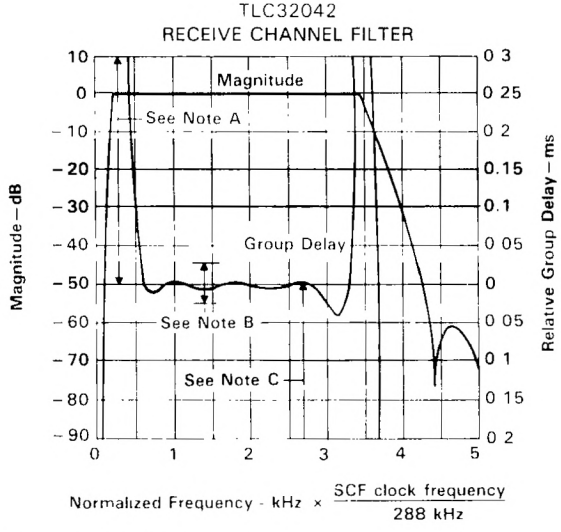
TLC32040 and TLC32041
RECEIVE CHANNEL FILTER



NOTES A. Maximum relative delay (200 Hz to 600 Hz) = 3350 μs
B. Maximum relative delay (600 Hz to 3000 Hz) = ±50 μs.
C. Absolute delay (600 Hz to 3000 Hz) = 1230 μs
D. Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions, SCF clock f = 288 kHz ±2%, input = ±3-V sinewave, and T_A = 25°C.

FIGURE 7

TYPICAL CHARACTERISTICS



NOTES: A. Maximum relative delay (200 Hz to 600 Hz) = 3350 μs
B. Maximum relative delay (600 Hz to 3000 Hz) = ±50 μs.
C. Absolute delay (600 Hz to 3000 Hz) = 1080 μs.
D. Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions, SCF clock f = 288 kHz ±2%, input = ±3-V sinewave, and T_A = 25°C

FIGURE 8

TYPICAL CHARACTERISTICS

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

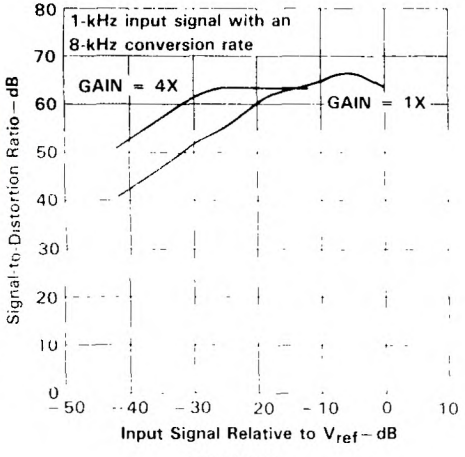


FIGURE 9

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0 dB INPUT SIGNAL)

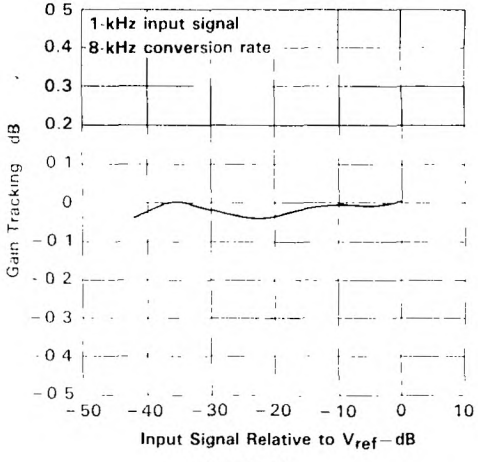


FIGURE 10

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

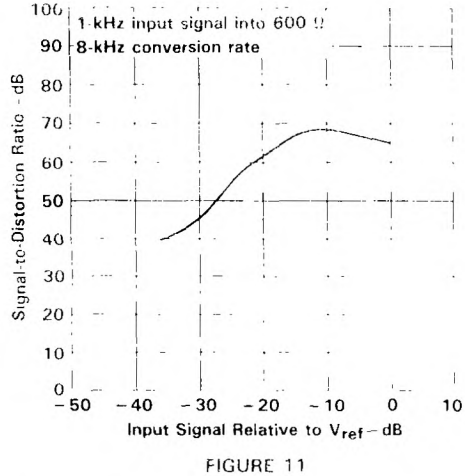


FIGURE 11

D/A GAIN TRACKING
vs
(GAIN RELATIVE TO GAIN
AT 0 dB INPUT SIGNAL)

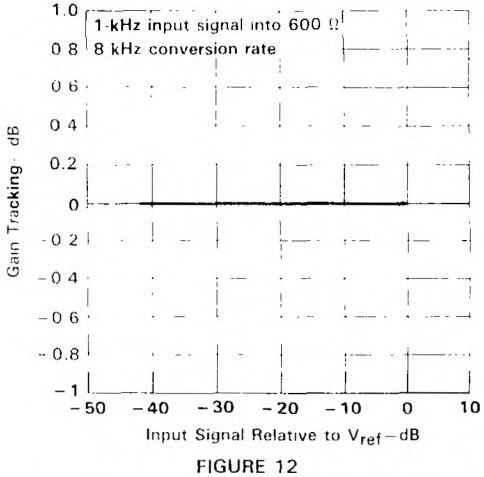


FIGURE 12

NOTE: Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions set clock f = 288 kHz ±2%, and T_A = 25°C.

TYPICAL CHARACTERISTICS

ATTENUATION OF SECOND HARMONIC OF A/D INPUT
vs
INPUT SIGNAL

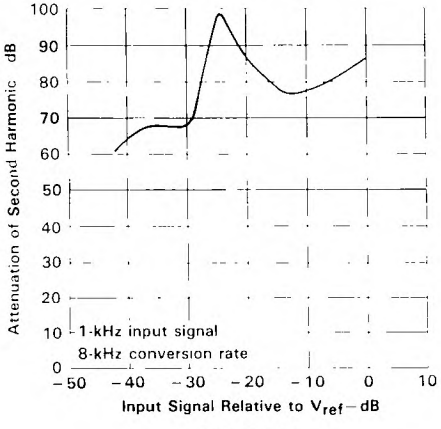


FIGURE 13

ATTENUATION OF THIRD HARMONIC OF A/D INPUT
vs
INPUT SIGNAL

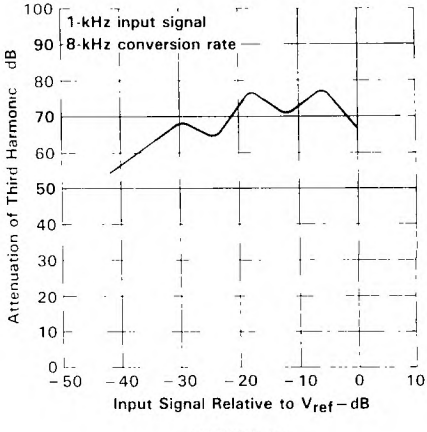


FIGURE 14

ATTENUATION OF SECOND HARMONIC OF D/A INPUT
vs
INPUT SIGNAL

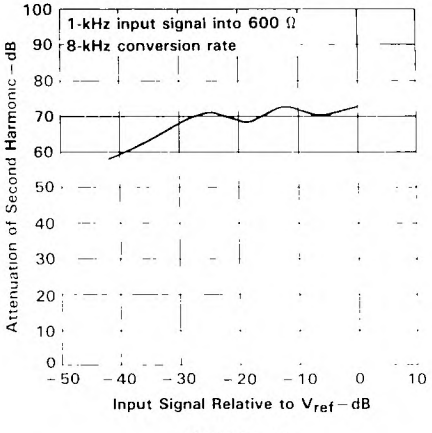


FIGURE 15

ATTENUATION OF THIRD HARMONIC OF D/A INPUT
vs
INPUT SIGNAL

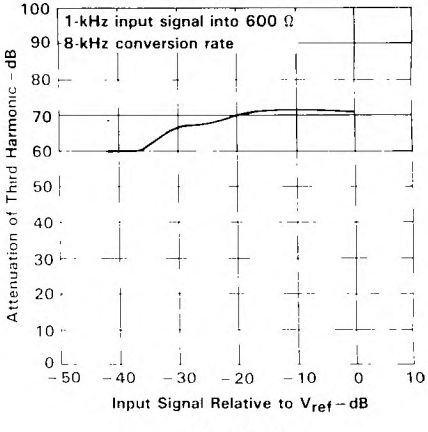
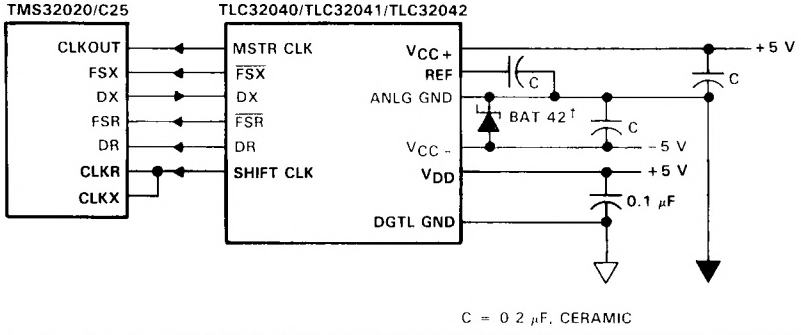


FIGURE 16

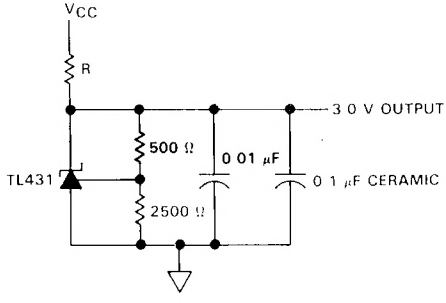
NOTE: Test conditions are V_{CC+}, V_{CC-}, and V_{DD} within recommended operating conditions set clock f = 288 kHz ±2%, and T_A = 25°C.

TYPICAL APPLICATION INFORMATION



C = 0.2 μF, CERAMIC

FIGURE 17. AIC INTERFACE TO THE TMS32020/C25 SHOWING DECOUPLING CAPACITORS AND SCHOTTKY DIODE†



FOR. V_{CC} = 12 V, R = 7200 Ω
V_{CC} = 10 V, R = 5600 Ω
V_{CC} = 5 V, R = 1600 Ω

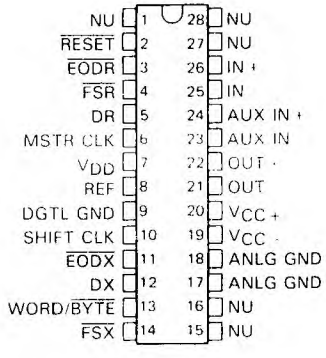
FIGURE 18. EXTERNAL REFERENCE CIRCUIT FOR TLC32041

†Thomson Semiconductors

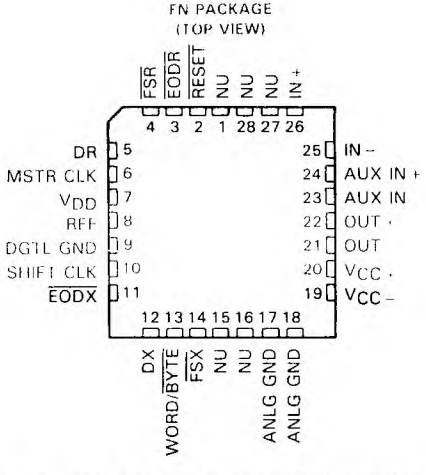
D3098, MARCH 1988 – REVISED DECEMBER 1988

- Advanced LinCMOS™ Silicon-Gate Process Technology
- 14-Bit Dynamic Range ADC and DAC
- 16-Bit Dynamic Range Input with Programmable Gain
- Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second
- Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter
- Serial Port for Direct Interface to TMS320C17, TMS32020, TMS320C25, and TMS320C30 Digital Processors
- Synchronous or Asynchronous ADC and DAC Conversion Rates with Programmable Incremental ADC and DAC Conversion Timing Adjustments
- Serial Port Interface to SN74299 Serial-to-Parallel Shift Register for Parallel Interface to TMS32010, TMS320C15, or Other Digital Processors
- Internal Reference for Normal Operation and External Purposes, or Can Be Overridden by External Reference

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NU – Nonusable; no external connection should be made to these pins. See Table 2.

description

The TLC32044 is a complete analog-to-digital and digital-to-analog input/output system on a single monolithic CMOS chip. This device integrates a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter. The device offers numerous combinations of Master Clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for this IC include speech encryption for digital transmission, speech recognition/storage systems, speech synthesis, modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS320C17, TMS32020, TMS320C25, and TMS320C30 digital signal

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description (continued)

processors, are provided. Also, when the transmit and receive sections of the Analog Interface Circuit (AIC) are operating synchronously, it will interface to two SN74299 serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the TMS32010, TMS320C15, other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of the IC can be selected and adjusted coincidentally with signal processing via software control.

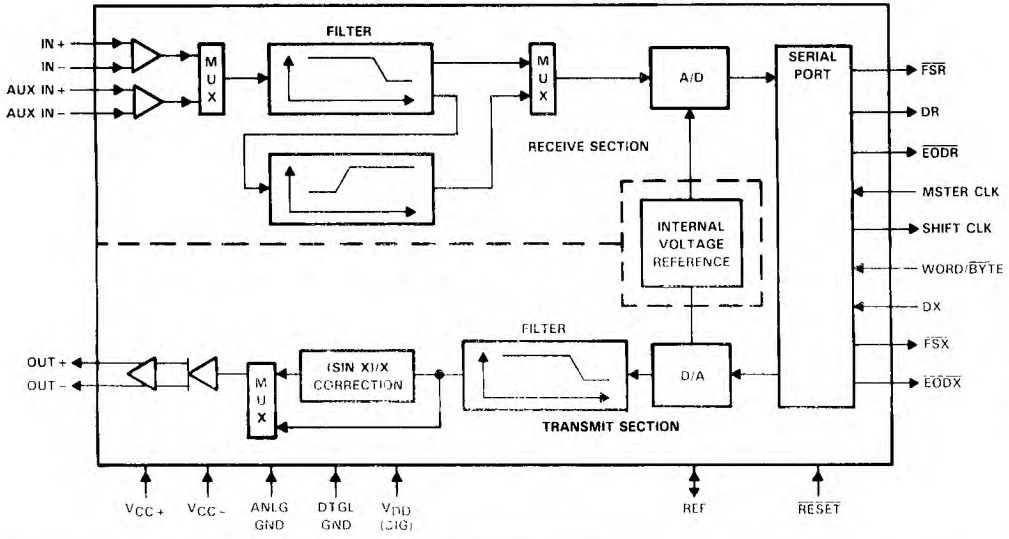
The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When only low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to a pin and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter) and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal. The on-board (sin x)/x correction filter can be switched out of the signal path using digital signal processor control, if desired.

The TLC32044I is characterized for operation from −40°C to 85°C, and the TLC32044C is characterized for operation from 0°C to 70°C.

functional block diagram



PRINCIPLES OF OPERATION

analog input

Two sets of analog inputs are provided. Normally, the IN+ and IN− input set is used; however, the auxiliary input set, AUX IN+ and AUX IN−, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN+, IN−, AUX IN+, and AUX IN− inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D bandpass filter, A/D bandpass filter clocking, and A/D conversion timing

The A/D high-pass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz and the A/D sample rate is 8 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz. The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 150 and 100 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 8 kHz.

The Internal Timing Configuration and AIC DX Data Word Format sections of this data sheet indicate the many options for attaining a 288-kHz bandpass switched-capacitor filter clock. These sections indicate that the RX Counter A can be programmed to give a 288-kHz bandpass switched-capacitor filter clock for several Master Clock input frequencies.

PRINCIPLES OF OPERATION (continued)

The A/D conversion rate is then attained by frequency-dividing the 288-kHz bandpass switched-capacitor filter clock with the RX Counter B. Thus, unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the bandpass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample-and-hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output of the (sin x)/x filter to eliminate the periodic sample data signal information, which occurs at multiples of the 288-kHz switched-capacitor filter clock. The continuous time filter also greatly attenuates any switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 288-kHz switched-capacitor filter clock with TX Counter B. Thus, unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (bandpass filter and ADC) are operated asynchronously, the low-pass and bandpass filter clocks are independently generated from the Master Clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and bandpass filters. In synchronous operation, the A/D conve timing is derived from, and is equal to, the D/A conversion timing. (See description of the WORD/$\overline{B}$ · ' pin in the Pin Functional Description Section.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample-and-hold that is realized with a switched-capacitor ladder.

system frequency response correction

(Sin x)/x correction for the D/A converter's zero-order sample-and-hold output can be provided by an on-board second-order (sin x)/x correction filter. This (sin x)/x correction filter can be inserted into or deleted from the signal path by digital signal processor control. When inserted, the (sin x)/x correction filter follows the switched-capacitor low-pass filter. When the TB register (see Internal Timing Configuration section) equals 36, the correction results of Figures 11 and 12 will be obtained.

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PRINCIPLES OF OPERATION (continued)

(Sin x)/x correction can also be accomplished by deleting the on-board second-order correction filter and performing the (sin x)/x correction in digital signal processor software. The system frequency response can be corrected via DSP software to ±0.1 dB accuracy to a band-edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (sin x)/x Correction Section for more details).

serial port

The serial port has four possible modes that are described in detail in the Functional Pin Description Section. These modes are briefly described below and in the Functional Description for Pin 13, WORD/$\overline{\text{BYTE}}$.

1. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS320C17.
2. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, and the TMS320C30.
3. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS320C17.
4. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, TMS320C30, or two SN74299 serial-to-parallel shift registers, which can then interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry.

operation of TLC32044 with internal voltage reference

The internal reference of the TLC32044 eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete control over the performance of the IC. The internal reference is brought out to a pin and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor may be connected between REF and ANLG GND.

operation of TLC32044 with external voltage reference

The REF pin may be driven from an external reference circuit if so desired. This external circuit must be capable of supplying 250 μA and must be adequately protected from noise such as crosstalk from the analog input.

reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset fun · will initialize all AIC registers, including the control register. After a negative-going pulse on the $\overline{\text{ET}}$ pin, the AIC will be initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section).

PRINCIPLES OF OPERATION (continued)

loopback

This feature allows the user to test the circuit remotely. In loopback, the OUT + and OUT – pins are internally connected to the IN + and IN – pins. Thus, the DAC bits (d15 to d2), which are transmitted to the DX pin, can be compared with the ADC bits (d15 to d2), which are received from the DR pin. An ideal comparison would be that the bits on the DR pin equal the bits on the DX pin. However, in practice there will be some difference in these bits due to the ADC and DAC output offsets.

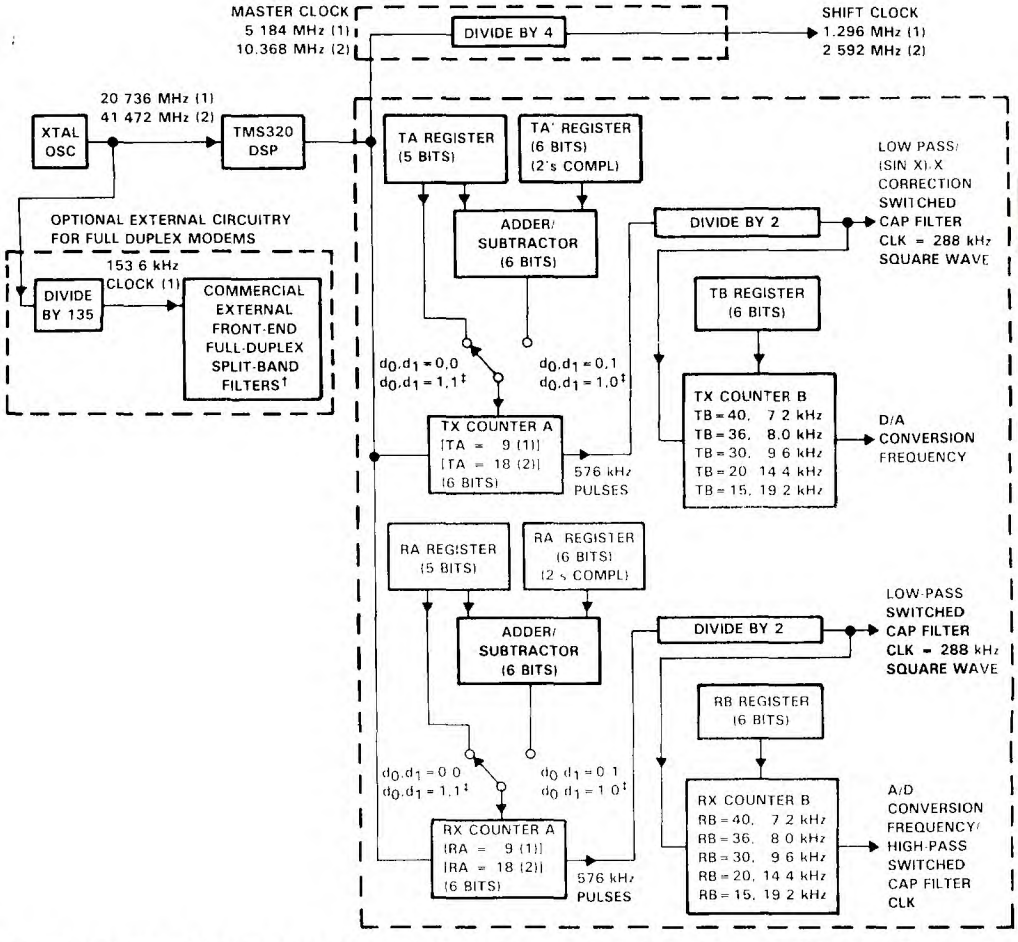
The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC Data Word Format section).

PIN NAME	PIN NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN +	24	I	Noninverting auxiliary analog input stage. This input can be switched into the bandpass filter and A/D converter path via software control. If the appropriate bit in the Control register is a 1, the auxiliary inputs will replace the IN + and IN – inputs. If the bit is a 0, the IN + and IN – inputs will be used (see the AIC DX Data Word Format section).
AUX IN –	23	I	Inverting auxiliary analog input (see the above AUX IN + pin description).
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	This pin is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	This pin is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port to the AIC is synchronized with the SHIFT CLK signal.
$\overline{\text{EODR}}$	3	O	(See the WORD/$\overline{\text{BYTE}}$ pin description and the Serial Port Timing Diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.

PIN NAME	PIN NO.	I/O	DESCRIPTION
$\overline{EODX}$	11	O	(See the WORD/$\overline{BYTE}$ pin description and the Serial Port Timing Diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the TMS320 serial port to the AIC. This signal can be used to interrupt a microprocessor upon the completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
$\overline{FSR}$	4	O	In the serial transmission modes, which are described in the WORD/$\overline{BYTE}$ pin description, the $\overline{FSR}$ pin is held low during bit transmission. When the $\overline{FSR}$ pin goes low, the TMS320 serial port will begin receiving bits from the AIC via the DR pin of the AIC. The most significant DR bit will be present on the DR pin before $\overline{FSR}$ goes low. (See Serial Port Timing and Internal Timing Configuration Diagrams.)
$\overline{FSX}$	14	O	When this pin goes low, the TMS320 serial port will begin transmitting bits to the AIC via the DX pin of the AIC. In all serial transmission modes, which are described in the WORD/$\overline{BYTE}$ pin description, the $\overline{FSX}$ pin is held low during bit transmission (see Serial Port Timing and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN−	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The Master Clock signal is used to derive all the key logic signals of the AIC, such as the Shift Clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the Master Clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters (see the Internal Timing Configuration)
OUT+	22	O	Noninverting output of analog output power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT−	21	O	Inverting output of analog output power amplifier. Functionally identical with and complementary to OUT+.
REF	8	I/O	The internal voltage reference is brought out on this pin. An external voltage reference can also be applied to this pin.
$\overline{RESET}$	2	I	A reset function is provided to initialize the TA, TA', TB, RA, RA', RB, and control registers. This reset function initiates serial communications between the AIC and DSP. The reset function will initialize all AIC registers including the control register. After a negative-going pulse on the $\overline{RESET}$ pin, the AIC registers will be initialized to provide an 8-kHz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', will be reset to 1. The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section). d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1 This initialization allows normal serial-port communication to occur between AIC and DSP.
SHIFT CLK	10	O	The Shift Clock signal is obtained by dividing the Master Clock signal frequency by four. This signal is used to clock the serial data transfers of the AIC, described in the WORD/$\overline{BYTE}$ pin description below (see the Serial Port Timing and Internal Timing Configuration diagram).
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage −5 V ±5%

PIN NAME	NO.	I/O	DESCRIPTION
WORD/$\overline{\text{BYTE}}$	13	I	This pin, in conjunction with a bit in the CONTROL register, is used to establish one of four serial modes These four serial modes are described below. *AIC transmit and receive sections are operated asynchronously* The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the Control register is a 0 (see the AIC DX Data Word Format), the transmit and receive sections will be asynchronous. L Serial port directly interfaces with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams). 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought low. 4. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin emits a positive frame-sync pulse that is four Shift Clock cycles wide. 5 One 8-bit byte is transmitted or one 8-bit byte is received. 6 The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought high. 7. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high H Serial port directly interfaces with the serial ports of the TMS32020, TMS320C25, and TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams) 1 The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low 2 One 16-bit word is transmitted or one 16-bit word is received 3. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin emits a low-going pulse. *AIC transmit and receive sections are operated synchronously.* If the appropriate data bit in the Control register is a 1, the transmit and receive sections will be configured to be synchronous. In this case, the bandpass switched-capacitor filter and the A/D conversion timing will be derived from the TX Counter A, TX Counter B, and TA, TA', and TB registers, rather than the RX Counter A, RX Counter B, and RA, RA', and RB registers. In this case, the AIC $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ timing will be identical during primary data communication; however, $\overline{\text{FSR}}$ will not be asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Serial Port Timing diagrams). L Serial port directly interfaces with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3 The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought low. 4 The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins emit positive frame-sync pulses that are four Shift Clock cycles wide. 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought high. 7. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high H Serial port directly interfaces with the serial ports of the TMS32020, TMS320C25, and TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams) 1 The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low 2. One 16-bit word is transmitted and one 16-bit word is received. 3 The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pins emit low-going pulses. Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port, with additional NOR and AND gates, will interface to two SN74299 serial-to-parallel shift registers. Interfacing the AIC to the SN74299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel, data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Serial Port Timing diagrams).

INTERNAL TIMING CONFIGURATION



NOTE: Frequency 1, 20.736 MHz, is used to show how 153.6 kHz (for a commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2, 41.472 MHz, is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.

†Split-band filtering can alternatively be performed after the analog input function via software in the TMS320.

‡These control bits are described in the AIC DX Data Word Format section.

explanation of internal timing configuration

All of the internal timing of the AIC is derived from the high-frequency clock signal that drives the Master Clock input pin. The Shift Clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the Master Clock input signal frequency by four.

Low-pass:

$$\text{SCF Clock Frequency (D/A or A/D Path)} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency (D/A or A/D Path)}}{\text{Contents of Counter B}}$$

High-pass:

$$\text{SCF Clock Frequency (A/D Path)} = \text{A/D Conversion Frequency}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master Clock Frequency}}{4}$$

TX Counter A and TX Counter B, which are driven by the Master Clock signal, determine the D/A conversion timing. Similarly, RX Counter A and RX Counter B determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path to meet its transfer function specifications, the frequency of its clock input must be 288 kHz. If the clock frequency is not 288 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 288 kHz. Thus, to obtain the specified filter response, the combination of Master Clock frequency and TX Counter A and RX Counter A values must yield a 288-kHz switched-capacitor clock signal. This 288-kHz clock signal can then be divided by the TX Counter B to establish the D/A conversion timing.

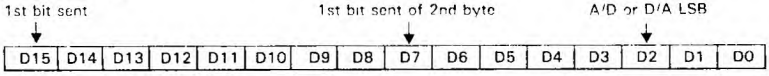
The transfer function of the bandpass switched-capacitor filter in the A/D path is a composite of its high-pass and low-pass section transfer functions. The high-frequency roll-off of the low-pass section will meet the bandpass filter transfer function specification when the low-pass section SCF is 288 kHz. Otherwise, the high-frequency roll-off will be frequency-scaled by the ratio of the high-pass section's SCF clock to 288 kHz. The low-frequency roll-off of the high-pass section will meet the bandpass filter transfer function specification when the A/D conversion rate is 8 kHz. Otherwise, the low-frequency roll-off of the high-pass section will be frequency-scaled by the ratio of the A/D conversion rate to 8 kHz.

TX Counter A and TX Counter B are reloaded every D/A conversion period, while RX Counter A and RX Counter B are reloaded every A/D conversion period. The TX Counter B and RX Counter B are loaded with the values in the TB and RB Registers, respectively. Via software control, the TX Counter A can be loaded with either the TA Register, the TA Register less the TA' Register, or the TA Register plus the TA' Register. By selecting the TA Register less the TA' Register option, the upcoming conversion timing will occur earlier by an amount of time that equals TA' times the signal period of the Master Clock. By selecting the TA Register plus the TA' Register option, the upcoming conversion timing will occur later by an amount of time that equals TA' times the signal period of the Master Clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX Counter A can be programmed via software control with the RA Register, the RA Register less the RA' Register, or the RA Register plus the RA' Register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the *transmit* and receive sections are configured to be synchronous (see WORD/$\overline{\text{BYTE}}$ pin description), then both the low-pass and bandpass switched-capacitor filter clocks are derived from TX Counter A. Also, both the D/A and A/D conversion timing are derived from the TX Counter A and TX Counter B. When the transmit and receive sections are configured to be synchronous, the RX Counter A, RX Counter B, RA Register, RA' Register, and RB Registers are not used.

AIC DR or DX word bit pattern



AIC DX data word format section

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	COMMENTS
primary DX serial communication protocol																
← d15 (MSB) through d2 go to the D/A converter register →														0	0	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with TB and RB register values.
← d15 (MSB) through d2 go to the D/A converter register →														0	1	The TX and RX Counter A's are loaded with the TA + TA' and RA + RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 0, d0 = 1 will cause the next D/A and A/D conversion periods to be changed by the addition of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1 AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →														1	0	The TX and RX Counter A's are loaded with the TA − TA' and RA − RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 1, d0 = 0 will cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →														1	1	The TX and RX Counter A's are loaded with the TA and RA register converter register values. The TX and RX Counter B's are loaded with the TB and RB register values. After a delay of four Shift Clock cycles, a secondary transmission will immediately follow to program the AIC to operate in the desired configuration.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (Primary Communications) to the AIC will initiate Secondary Communications upon completion of the Primary Communications

Upon completion of the Primary Communication, $\overline{\text{FSX}}$ will remain high for four SHIFT CLOCK cycles and will then go low and initiate the Secondary Communication. The timing specifications for the Primary and Secondary Communications are identical. In this manner, the Secondary Communication, if initiated, is interleaved between successive Primary Communications. This interleaving prevents the Secondary Communication from interfering with the Primary Communications and DAC timing, thus preventing the AIC from skipping a DAC output. It is important to note that in the synchronous mode, $\overline{\text{FSR}}$ will not be asserted during Secondary Communications.

secondary DX serial communication protocol

x x | ← to TA register → | x x | ← to RA register → | 0 0	d13 and d6 are MSBs (unsigned binary)
x | ← to TA' register → | x | ← to RA' register → | 0 1	d14 and d7 are 2's complement sign bits
x | ← to TB register → | x | ← to RB register → | 1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x d9 x d7 d6 d5 d4 d3 d2 1 1 CONTROL REGISTER	d2 = 0/1 deletes/inserts the A/D high-pass filter d3 = 0/1 disables/enables the loopback function d4 = 0/1 disables/enables the AUX IN+ and AUX IN− pins d5 = 0/1 asynchronous/synchronous transmit and receive sections d6 = 0/1 gain control bits (see Gain Control Section) d7 = 0/1 gain control bits (see Gain Control Section) d9 = 0/1 delete/insert on-board second-order (sin x)/x correction filter

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function will initialize all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on the $\overline{\text{RESET}}$ pin will initialize the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184 MHz master clock input signal. The AIC, excepting the CONTROL register, will be initialized as follows (see AIC DX Data Word Format section):

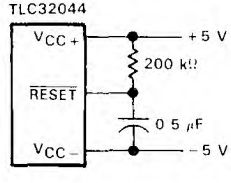
REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA'	1
TB	24
RA	9
RA'	1
RB	24

The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section):

d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA', and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the Pin Descriptions and AIC DX Word Format sections).

The circuit shown below will provide a reset on power-up when power is applied in the sequence given under Power-Up Sequence. The circuit depends on the power supplies' reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.



power-up sequence

To ensure proper operation of the AIC, and as a safeguard against latch-up, it is recommmended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND (see Figure 21). In the absence of such diodes, power should be applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal should be applied until after power-up.

AIC responses to improper conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 1 below.

AIC register constraints

The following constraints are placed on the contents of the AIC registers:

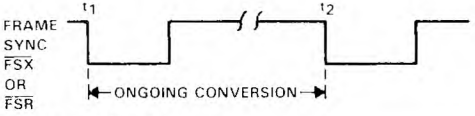
1. TA register must be > 1.
2. TA' register can be either positive, negative, or zero.
3. RA register must be > 1.
4. RA' register can be either positive, negative, or zero.
5. (TA register ± TA' register) must be > 1.
6. (RA register ± RA' register) must be > 1.
7. TB register must be > 1.

TABLE 1. AIC RESPONSES TO IMPROPER CONDITIONS

IMPROPER CONDITION	AIC RESPONSE
TA register + TA' register = 0 or 1 TA register − TA' register = 0 or 1	Reprogram TX Counter A with TA register value
TA register + TA' register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into the TX Counter A, i.e., TA register + TA' register + 40 HEX is loaded into TX Counter A
RA register + RA' register = 0 or 1 RA register − RA' register = 0 or 1	Reprogram RX Counter A with RA register value
RA register + RA' register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX Counter A, i.e., RA register + RA' register + 40 HEX is loaded into RX Counter A
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down
TB register = 0 or 1	Reprogram TB register with 24 HEX
RB register = 0 or 1	Reprogram RB register with 24 HEX
AIC and DSP cannot communicate	Hold last DAC output

improper operation due to conversion times being too close together

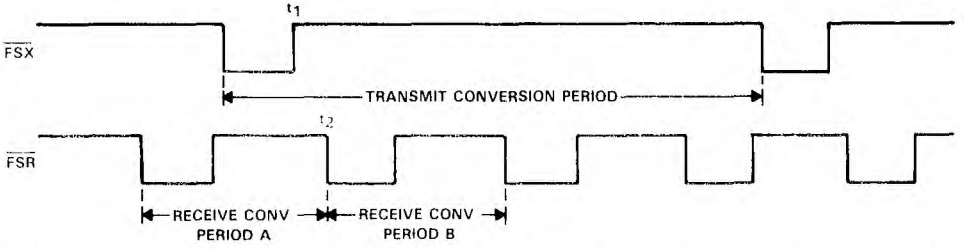
If the difference between two successive D/A conversion frame syncs is less that 1/19.2 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A' register or A − A' register result is too small. When incrementally adjusting the conversion period via the A + A' register options, the designer should be very careful not to violate this requirement (see diagram below).



$t_2 - t_1 \geq 1/19.2$ kHz

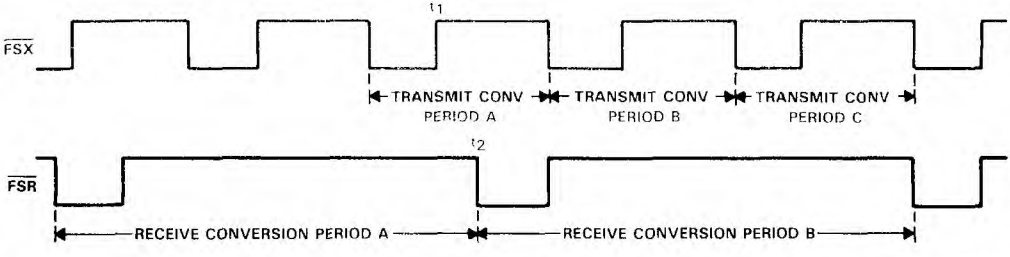
asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing conversion period is then adjusted. However, either Receive Conversion Period A or B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t1 and t2, the receive conversion period adjustment will be performed during Receive Conversion Period A. Otherwise, the adjustment will be performed during Receive Conversion Period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see figure below).



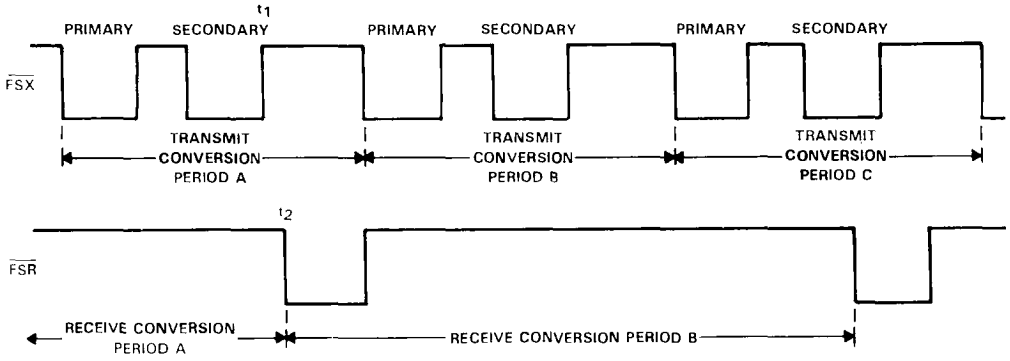
asynchronous operation — more than one transmit frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the figure below. If the adjustment command is issued during Transmit Conversion Period A, Receive Conversion Period A will be adjusted if there is sufficient time between t1 and t2. Or, if there is not sufficient time between t1 and t2, Receive Conversion Period B will be adjusted. Or, the receive portion of an adjustment command may be ignored if the adjustment command is sent during a receive conversion period, which is already being or will be adjusted due to a prior adjustment command. For example, if adjustment commands are issued during Transmit Conversion Periods A, B, and C, the first two commands may cause Receive Conversion Periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during Receive Conversion Period B, which already will be adjusted via the Transmit Conversion Period B adjustment command.



asynchronous operation – more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX Data Word Format section)

The TA, TA', TB, and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t1 and t2, the TA, RA', and RB register information, which is sent during Transmit Conversion Period A, will be applied to Receive Conversion Period A. Otherwise, this information will be applied during Receive Conversion Period B. If RA, RA', and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA, RA', or RB information that is received during this receive conversion period will be disregarded (see diagram below).



test modes†

The following paragraph provides information that allows the TLC32044 to be operated in special test modes. These test modes are used by Texas Instruments to facilitate testing of the device during manufacturing. They are not intended to be used in real applications, however, they allow the filters in the A/D and D/A paths to be used without using the A/D and D/A converters.

In normal operation, the nonusable (NU) pins are left unconnected. These NU pins are used by the factory to speed up testing of the TLC32044 Analog Interface Circuit (AIC). When the device is used in normal (non-test-mode) operation, the NU pin (pin 1) has an internal pull-down to −5 V. Externally connecting 0 V or 5 V to pin 1 puts the device in test-mode operation. Selecting one of the possible test modes is accomplished by placing a particular voltage on certain pins. A description of these modes is provided in Table 2 and Figures 1 and 2.

TABLE 2. LIST OF TEST MODES

TEST PINS	D/A PATH TEST (PIN 1 to 5 V)	A/D PATH TEST (PIN 1 to 0)
	TEST FUNCTION	TEST FUNCTION
5	The low-pass switched-capacitor filter clock is brought out to pin 5. This clock signal is normally internal.	The bandpass switched-capacitor filter clock is brought out to pin 5. This clock signal is normally internal.
11	No change from normal operation. The $\overline{\text{EODX}}$ signal is brought out to pin 11.	The pulse that initiates the A/D conversion is brought out here. This signal is normally internal.
3	The pulse that initiates the D/A conversion is brought out here.	No change from normal operation. The EODR signal is brought out.
27 and 28	There are no test output signals provided on these pins.	The outputs of the A/D path low-pass or bandpass filter (depending upon control bit d2 — see AIC DX Data Word Format section) are brought out to these pins. If the high-pass section is inserted, the output will have a (sinx)/x droop. The slope of the droop will be determined by the ADC sampling frequency, which is the high-pass section clock frequency (see diagram of bandpass or low-pass filter test for receive section). These outputs will drive small (30-pF) loads.
	D/A PATH LOW-PASS FILTER TEST; PIN 13 (WORD/$\overline{\text{BYTE}}$) to −5 V	
	TEST FUNCTION	
15 and 16	The inputs of the D/A path low-pass filter are brought out to pins 15 and 16. The D/A input to this filter is removed. If the (sin x)/x correction filter is inserted, the OUT+ and OUT− signals will have a flat response (see Figure 2). The common-mode range of these inputs must not exceed ±0.5 V	

† In the test mode, the AIC responds to the setting of Pin 13 to −5 V, as if Pin 13 were set to 0 V. Thus, the byte mode is selected for communicating between DSP and AIC. Either of the path tests (D/A or A/D) can be performed simultaneously with the D/A low-pass filter test. In this situation, Pin 13 must be connected to −5 V, which initiates byte-mode communications.

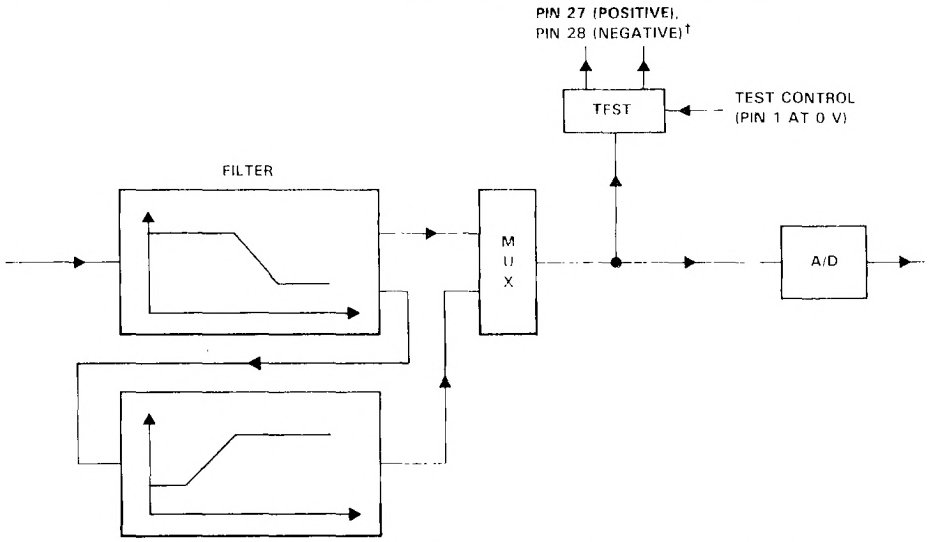


FIGURE 1. BANDPASS OR LOW-PASS FILTER TEST FOR RECEIVER SECTION

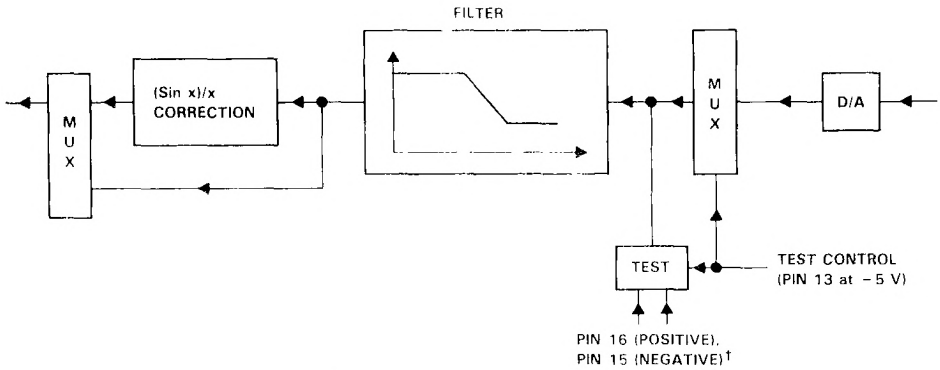


FIGURE 2. LOW-PASS FILTER TEST FOR TRANSMIT SECTION

†All analog signal paths have differential architecture and hence have positive and negative components

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . −0.3 V to 15 V
Supply voltage, V_{DD} . . . . . −0.3 V to 15 V
Output voltage, V_O . . . . . −0.3 V to 15 V
Input voltage, V_I . . . . . −0.3 V to 15 V
Digital ground voltage . . . . . −0.3 V to 15 V
Operating free-air temperature range: TLC32044I . . . . . −40°C to 85°C
TLC32044C . . . . . 0°C to 70°C
Storage temperature range . . . . . −40°C to 125°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: Voltage values for maximum ratings are with respect to VCC−.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 3)		−0.3		0.8	V
Load resistance at OUT+ and/or OUT−, R_L		300			Ω
Load capacitance at OUT+ and/or OUT−, C_L				100	pF
MSTR CLK frequency (see Note 4)		0.075	5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				19.2	kHz
Conversion rate				20	kHz
Operating free-air temperature, T_A	TLC32044I	−40		85	°C
	TLC32044C	0		70	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-}, are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.
4. The bandpass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 8 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF clock is shifted from 8 kHz, the high-pass roll-off frequency will shift by the ratio of the high-pass SCF clock to 8 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the SCF clock to 288 kHz
5. This range applies when (IN+ − IN−) or (AUX IN+ − AUX IN−) equals ±6 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC32044I				40	mA
		TLC32044C				35	
I_{CC-}	Supply current from V_{CC-}	TI [illegible]4I				−40	mA
		TI [illegible]4C				−35	
I_{DD}	Supply current from V_{DD}		$f_{MSTR\ CLK}$ = 5.184 MHz			7	mA
V_{ref}	Internal reference output voltage			3		3.3	V
αV_{ref}	Temperature coefficient of internal reference vc				250		ppm/°C
r_o	Output resistance at ·				100		kΩ

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters in)			10	70	mV
CMRR	Common-mode rejection ratio at IN+, IN−, or AUX IN+, AUX IN−	See Note 6		55		dB
r_I	Input resistance at IN+, IN− or AUX IN+, AUX IN−, REF			100		kΩ

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT− (single-ended relative to ANLG GND)			15	80	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT− (single-ended)	$R_L \geq 300\ \Omega$, Offset voltage = 0	±3			V
V_{OM}	Maximum peak output voltage swing between OUT+ and OUT− (differential output)	$R_L \geq 600\ \Omega$	±6			V

†All typical values are at T_A = 25°C

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with an 8-kHz conversion rate.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

system distortion specifications, SCF clock frequency = 288 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	V_{in} = −0.1 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended	V_{in} = −0.1 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	differential		57	65		
Attenuation of second harmonic of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	differential		57	65		

A/D channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	A_v = 1‡		A_v = 2‡		A_v = 4‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	58		>58§		>58§		dB
	V_{in} = −12 dB to −6 dB	58		58		>58§		
	V_{in} = −18 dB to −12 dB	56		58		58		
	V_{in} = −24 dB to −18 dB	50		56		58		
	V_{in} = −30 dB to −24 dB	44		50		56		
	V_{in} = −36 dB to −30 dB	38		44		50		
	V_{in} = −42 dB to −36 dB	32		38		44		
	V_{in} = −48 dB to −42 dB	26		32		38		
	V_{in} = −54 dB to −48 dB	20		26		32		

† All typical values are at T_A = 25°C.
‡ A_v is the programmable gain of the input amplifier.
§ A value >60 is over range and signal clipping occurs.

D/A channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	58		dB
	V_{in} = −12 dB to −6 dB	58		
	V_{in} = −18 dB to −12 dB	56		
	V_{in} = −24 dB to −18 dB	50		
	V_{in} = −30 dB to −24 dB	44		
	V_{in} = −36 dB to −30 dB	38		
	V_{in} = −42 dB to −36 dB	32		
	V_{in} = −48 dB to −42 dB	26		
	V_{in} = −54 dB to −48 dB	20		

NOTE 7: The test condition is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted) (Continued)

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Absolute transmit gain tracking error while transmitting into 600 Ω	−48 dB to 0 dB signal range, See Note 8		±0.05	±0.15	dB
Absolute receive gain tracking error	−48 dB to 0 dB signal range, See Note 8		±0.05	±0.15	dB

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single-ended)				80		dB

†All typical values are at T_A = 25°C.
NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

delay distortion

bandpass filter transfer function, SCF f_{clock} = 288 kHz, input (IN+ − IN−) is a ±3-V sinewave† (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f ≤ 50 Hz	K1 × 0 dB	−33	−29	−25	dB
		f = 100 Hz	K1 × 0.26 dB	−4	−2	−1	
		f = 150 Hz to 3100 Hz	K1 × 0 dB	−0.25	0	0.25	
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 3300 Hz to 3650 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB	−5	−3	−1	
		f = 4000 Hz	K1 × 2.7 dB	−20	−17	−16	
		f ≥ 4400 Hz	K1 × 3.2 dB			−40	
		f ≥ 5000 Hz	K1 × 0 dB			−65	

low-pass filter transfer function, SCF f_{clock} = 288 kHz (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f = 0 Hz to 3100 Hz	K1 × 0 dB		0	0.25	dB
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 3300 Hz to 3650 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB	−5	−3	−1	
		f = 4000 Hz	K1 × 2.7 dB	−20	−17	−16	
		f ≥ 4400 Hz	K1 × 3.2 dB			−40	
		f ≥ 5000 Hz	K1 × 0 dB			−65	

serial port

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 300 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	μA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† See filter curves in typical characteristics.

‡ The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 • [(SCF frequency − 288 kHz)/288 kHz]. For errors greater than 0.25%, see Note 10.

§ All typical values are at T_A = 25°C.

NOTES: 9. The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 150 to 3600 Hz and 0 to 3600 Hz for the bandpass and low-pass filters respectively.

10. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

noise (measurement includes low-pass and bandpass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
Transmit noise	with (sin x)/x	DX input = 00000000000000, constant input code		550	μV rms
	without (sin x)/x		325	425	μV rms
			18		dBrnc0
Receive noise (see Note 11)		Inputs grounded, gain = 1	300	500	μV rms
			18		dBrnc0

timing requirements

serial port recommended input signals

	PARAMETER	MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	$\overline{RESET}$ pulse duration (see Note 12)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
$t_{h(DX)}$	DX hold time after ↓	$t_{c(SCLK)}/4$		ns

†All typical values are at T_A = 25°C.

NOTES: 11. The noise is computed by statistically evaluating the digital output of the A/D converter.

12. $\overline{RESET}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (continued)

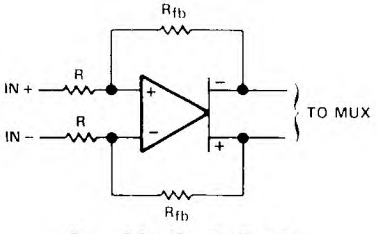
serial port — AIC output signals

PARAMETER		MIN	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		50	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		50	ns
	Shift clock (SCLK) duty cycle	45	55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to		90	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to FSR/$\overline{FSX}$↑		90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑		90	ns
$t_{dw(CH-EL)}$	Delay from SCLK↑ to $\overline{E}$	$\overline{R}$↓ in word mode	90	ns
$t_{dw(CH-EH)}$	from SCLK↑ to $\overline{EODX}$/$\overline{EODR}$↑ in word mode		90	ns
$t_{f(EODX)}$	fall time		15	ns
$t_{f(EODR)}$	$\overline{E}$ all time		15	ns
$t_{db(CH-EL)}$	Delay from SCLK↑ to $\overline{EO}$	in byte mode	100	ns
$t_{db(CH-EH)}$	Delay from SCLK↑ to $\overline{EO}$	in byte mode	100	ns

TABLE 2. GAIN CONTROL TABLE
(ANALOG INPUT SIGNAL REQUIRED FOR FULL-SCALE A/D CONVERSION)

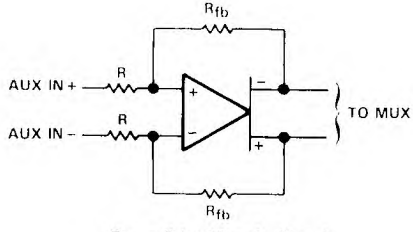
INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT†	A/D CONVERSION RESULT
	d6	d7		
Differential configuration	1	1	±6 V	full-scale
Analog input = IN+ − IN−	0	0		
= AUX IN+ − AUX IN−	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale
Single-ended configuration	1	1	±3 V	half-scale
Analog input = IN+ − ANLG GND	0	0		
AUX IN	ANLG GND	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale

† In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 3. IN+ AND IN− GAIN CONTROL CIRCUITRY



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0, d7 = 1

FIGURE 4. AUX IN+ AND AUX IN− GAIN CONTROL CIRCUITRY

(sin x)/x correction section

If the designer does not wish to use the on-board second-order (sin x)/x correction filter, correction can be accomplished in digital signal processor (DSP) software. (Sin x)/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown below, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the TMS320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction will add a slight amount of group delay at the upper edge of the 300–3000-Hz band.

(sin x)/x roll-off for a zero-order hold function

The (sin x)/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

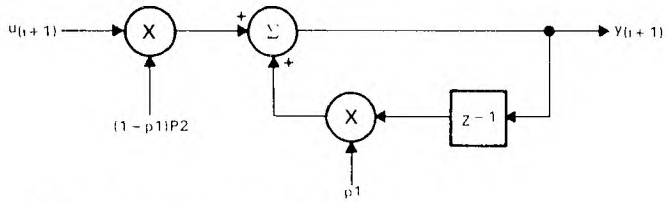
TABLE 3. (sin x)/x ROLL-OFF

f_S (Hz)	$20 \log \frac{\sin \pi f/f_S}{\pi f/f_S}$ (f = 3000 Hz) (dB)
7200	2.64
8000	2.11
9600	1.44
14400	0.63
19200	−0.35

Note that the actual AIC (sin x)/x roll-off will be slightly less than the above figures, because the AIC has less than a 100% duty cycle hold interval.

correction filter

To compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter shown below, is recommended.



The difference equation for this correction filter is:

$$y_{i+1} = p2(1-p1)(u_{i+1}) + p1\, y_i$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{p2^2 (1-p1)^2}{1 - 2p1 \cos(2\pi f/f_S) + p1^2}$$

correction results

Table 4 below shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates.

TABLE 4

f (Hz)	ERROR (dB) f_s = 8000 Hz p1 = −0.14813 p2 = 0 9888	ERROR (dB) f_s = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	0 099	0 043
600	0 089	0 043
900	0 054	0
1200	0 002	0
1500	0 041	0
1800	0 079	0 043
2100	0 100	0 043
2400	0 091	0 043
2700	0 043	0
3000	0 102	0 043

TMS320 software requirements

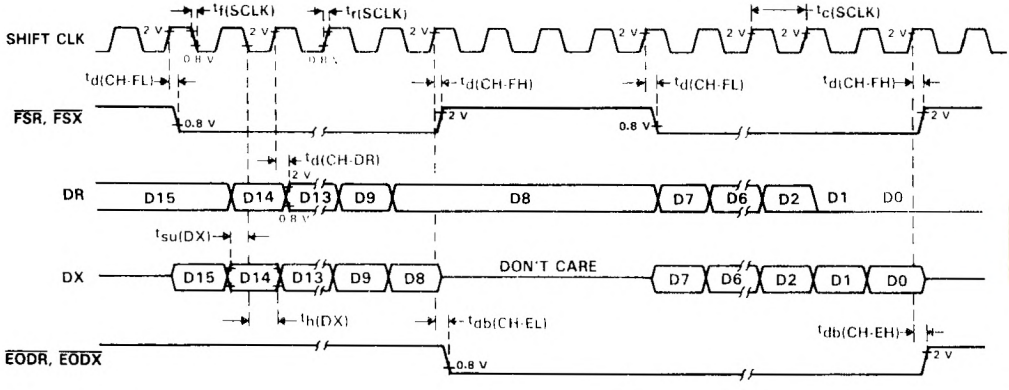
The digital correction filter equation can be written in state variable form as follows:

$$Y = k1Y + k2U$$

where k1 equals p1 (from the preceding page), k2 equals (1 − p1)p2 (from the preceding page), Y is the filter state, and U is the next I/O sample. The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) will yield the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

byte-mode timing



word-mode timing

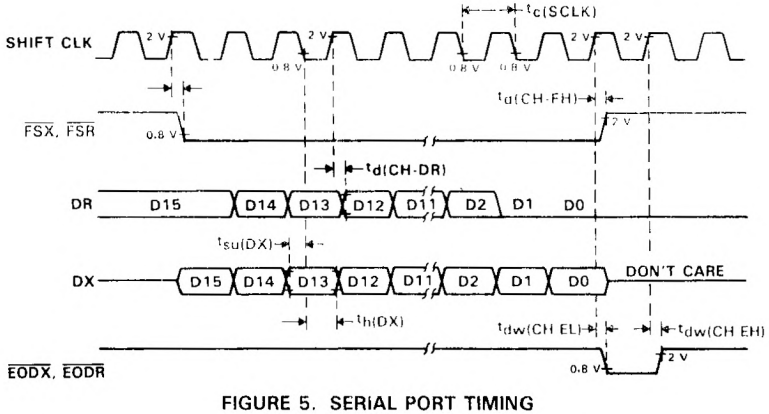


FIGURE 5. SERIAL PORT TIMING

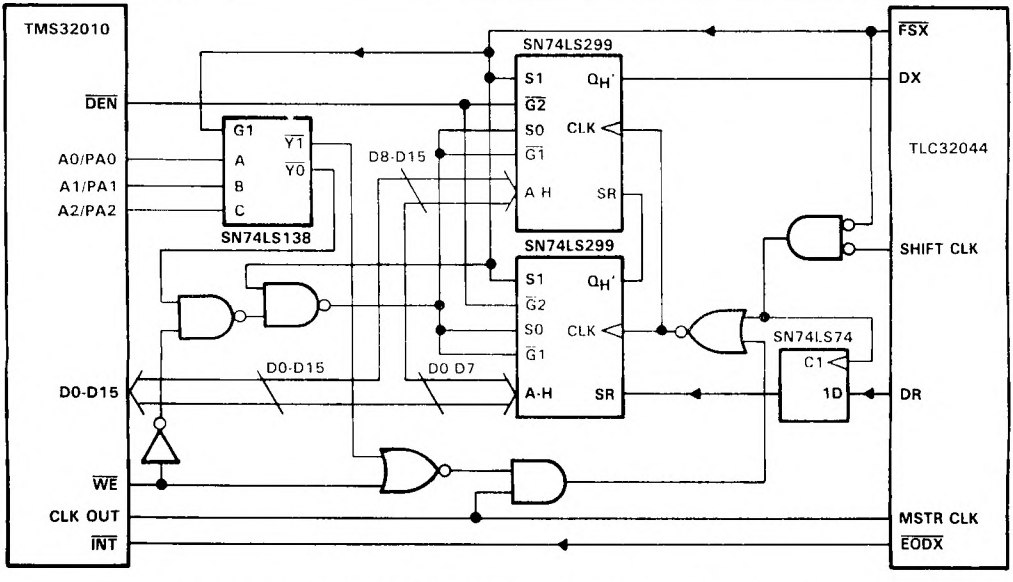
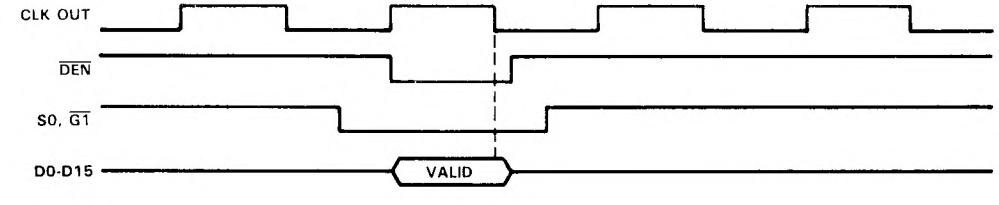


FIGURE 6. TMS32010/TMS320C15-TLC32044 INTERFACE CIRCUIT

in instruction timing



out instruction timing

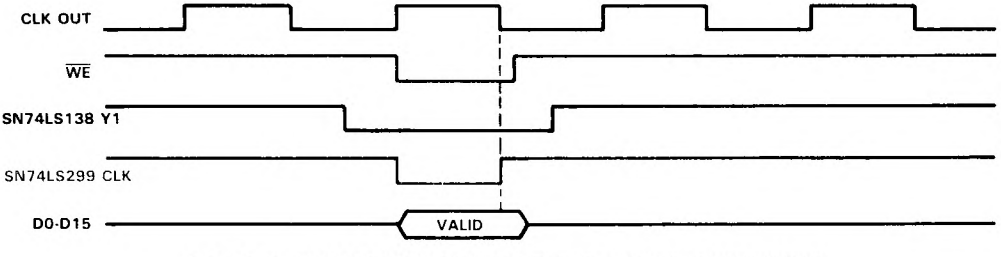


FIGURE 7. TMS32010/TMS320C15-TLC32044 INTERFACE TIMING

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

AIC TRANSMIT AND RECEIVE LOW-PASS FILTER

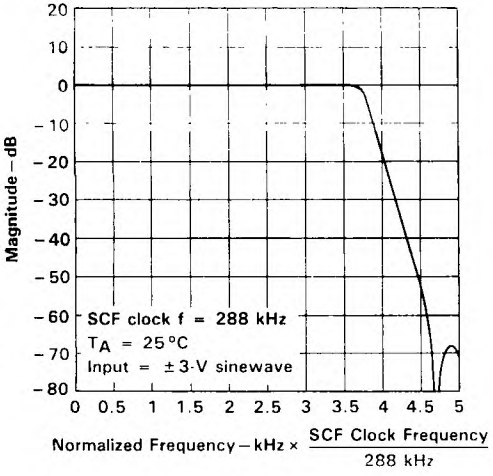


FIGURE 8

AIC TRANSMIT AND RECEIVE LOW-PASS FILTER

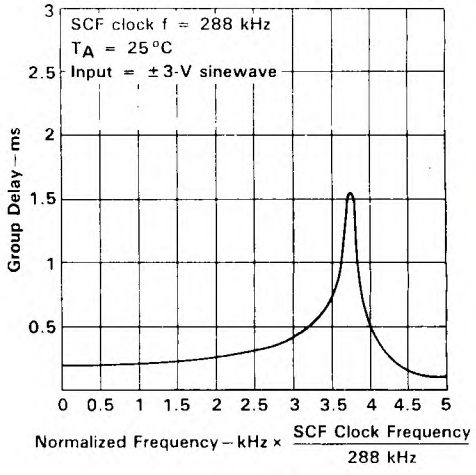


FIGURE 9

AIC RECEIVE-CHANNEL BANDPASS FILTER

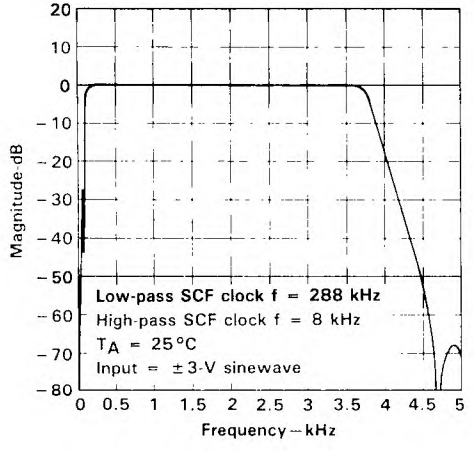


FIGURE 10

AIC RECEIVE-CHANNEL HIGH-PASS FILTER

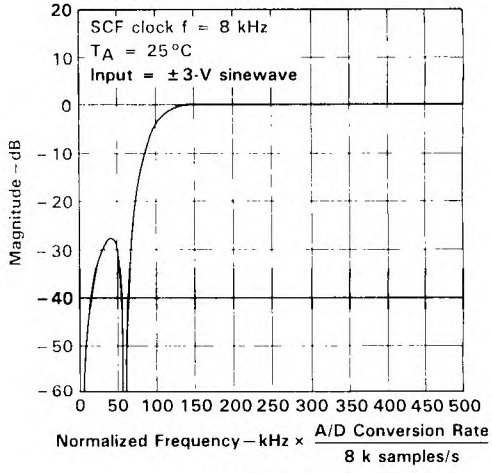


FIGURE 11

TYPICAL CHARACTERISTICS

AIC RECEIVE CHANNEL BANDPASS FILTER

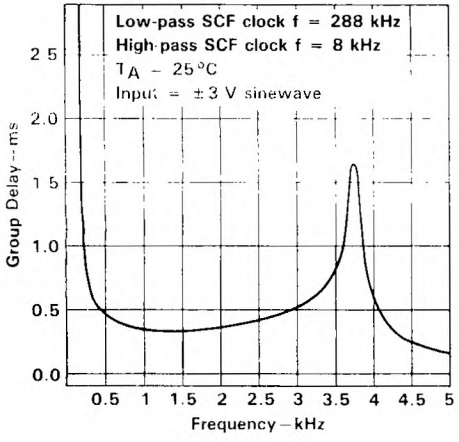


FIGURE 12

AIC (SIN X)/X CORRECTION FILTER

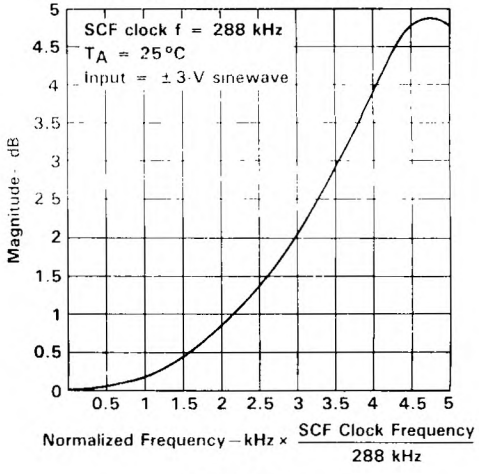


FIGURE 13

(SIN X) X CORRECTION FILTER

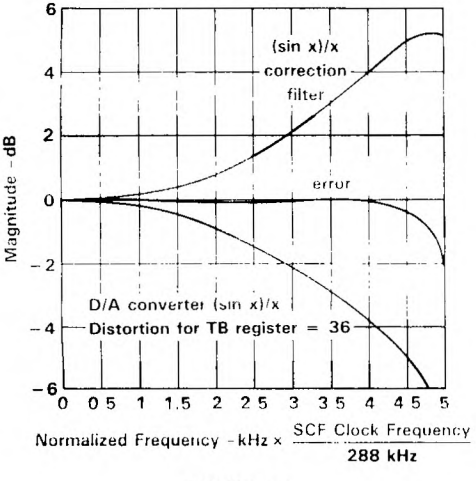


FIGURE 14

A D SIGNAL TO-DISTORTION RATIO
vs
INPUT SIGNAL

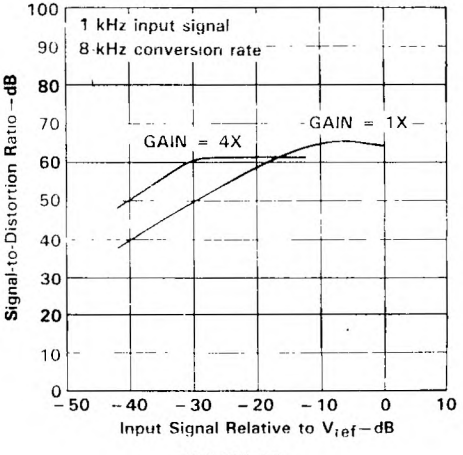


FIGURE 15

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN AT 0 dB INPUT SIGNAL)

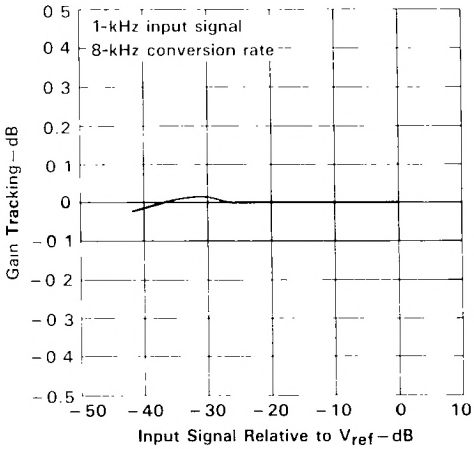


FIGURE 16

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL LEVEL

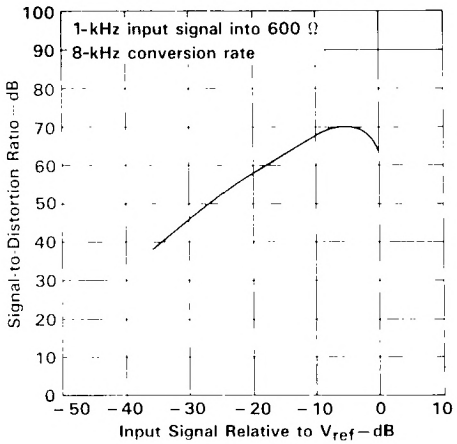


FIGURE 17

TYPICAL CHARACTERISTICS

D/A GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0 dB INPUT SIGNAL LEVEL)

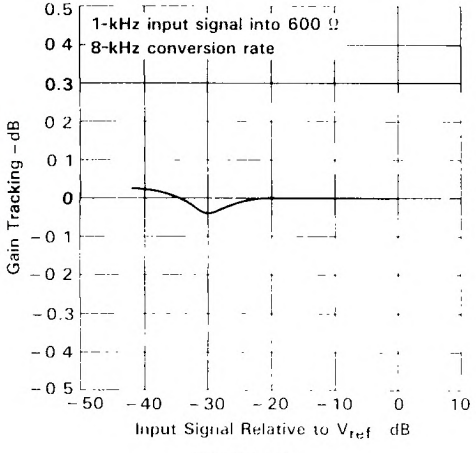


FIGURE 18

A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

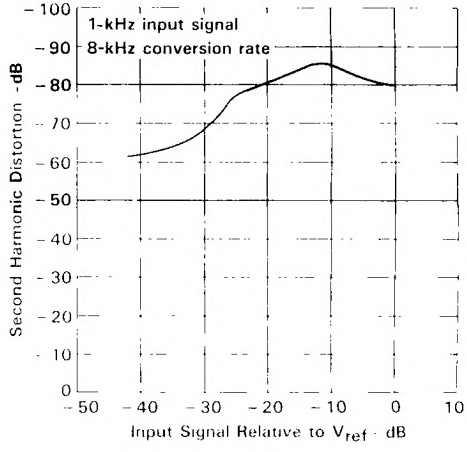


FIGURE 19

D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

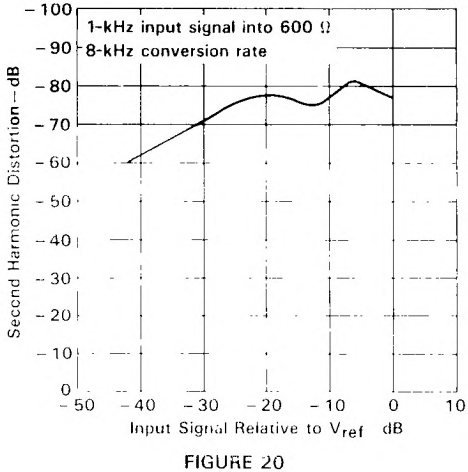


FIGURE 20

TYPICAL CHARACTERISTICS

A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

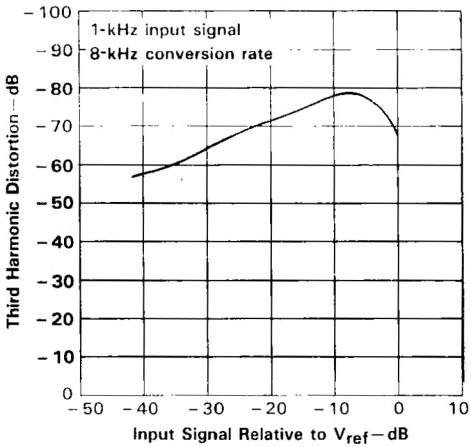


FIGURE 21

D.A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

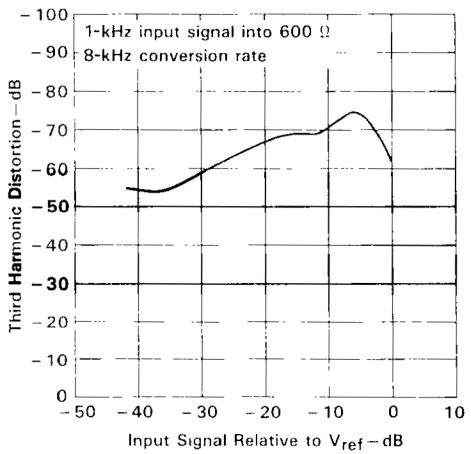
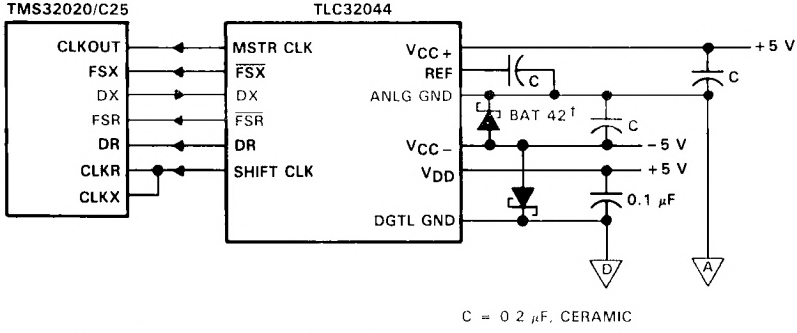


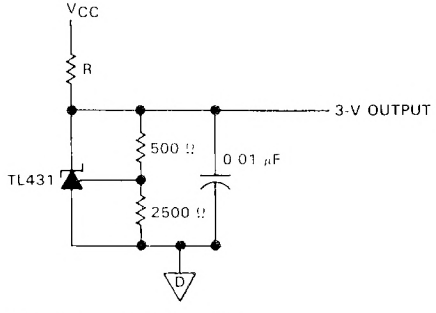
FIGURE 22

TYPICAL APPLICATION INFORMATION



C = 0.2 μF, CERAMIC

FIGURE 23. AIC INTERFACE TO THE TMS32020/C25 SHOWING DECOUPLING CAPACITORS AND SCHOTTKY DIODE†



FOR V_{CC} = 12 V, R = 7200 Ω
V_{CC} = 10 V, R = 5600 Ω
V_{CC} = 5 V, R = 1600 Ω

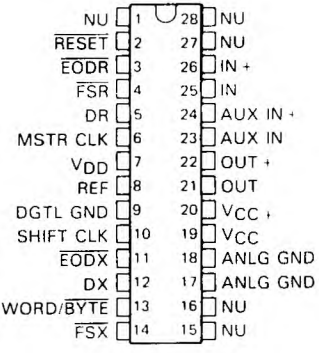
FIGURE 24. EXTERNAL REFERENCE CIRCUIT FOR TLC32044

† Thomson Semiconductors

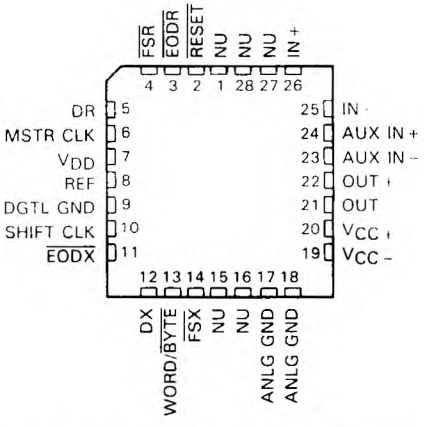
D3188, DECEMBER 1988

- Advanced LinCMOS™ Silicon-Gate Process Technology
- 14-Bit Dynamic Range ADC and DAC
- 16-Bit Dynamic Range Input with Programmable Gain
- Variable ADC and DAC Sampling Rate Up to 19,200 Samples per Second
- Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter
- Serial Port for Direct Interface to TMS320C17, TMS32020, TMS320C25, and TMS320C30 Digital Processors
- Synchronous or Asynchronous ADC and DAC Conversion Rates with Programmable Incremental ADC and DAC Conversion Timing Adjustments
- Serial Port Interface to SN74299 Serial-to-Parallel Shift Register for Parallel Interface to TMS32010, TMS320C15, or Other Digital Processors
- Internal Reference for Normal Operation and External Purposes, or Can Be Overridden by External Reference

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NU – Nonusable; no external connection should be made to these pins. See Table 2.

description

The TLC32045 is a complete analog-to-digital and digital-to-analog input/output system on a single monolithic CMOS chip. This device integrates a bandpass switched-capacitor antialiasing input filter, a 14-bit-resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit-resolution D/A converter, and a low-pass switched-capacitor output-reconstruction filter. The device offers numerous combinations of Master Clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for this IC include speech encryption for digital transmission, speech recognition/storage systems, speech synthesis, modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rate), analog interface for digital signal processors (DSPs), industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS320C17, TMS32020, TMS320C25, and TMS320C30 digital signal

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description (continued)

processors, are provided. Also, when the transmit and receive sections of the Analog Interface Circuit (AIC) are operating synchronously, it will interface to two SN74299 serial-to-parallel shift registers. These serial-to-parallel shift registers can then interface in parallel to the TMS32010, TMS320C15, other digital signal processors, or external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of the IC can be selected and adjusted coincidentally with signal processing via software control.

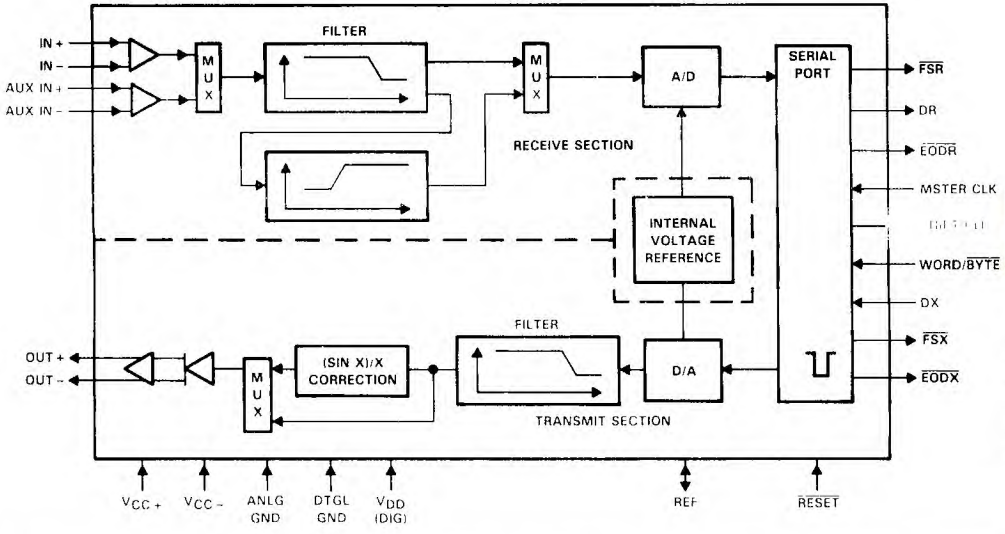
The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When only low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A converters each have 14 bits of resolution with 9 bits of integral linearity specified over any 9-bit range. The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to a pin and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter) and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal. The on-board (sin x)/x correction filter can be switched out of the signal path using digital signal processor control, if desired.

The TLC32045I is characterized for operation from $-40\,^{\circ}C$ to $85\,^{\circ}C$, and the TLC32045C is characterized for operation from $0\,^{\circ}C$ to $70\,^{\circ}C$.

functional block diagram



PRINCIPLES OF OPERATION

analog input

Two sets of analog inputs are provided. Normally, the IN+ and IN− input set is used; however, the auxiliary input set, AUX IN+ and AUX IN−, can be used if a second input is required. Each input set can be operated in either differential or single-ended modes, since sufficient common-mode range and rejection are provided. The gain for the IN+, IN−, AUX IN+, and AUX IN− inputs can be programmed to be either 1, 2, or 4 (see Table 2). Either input circuit can be selected via software control. It is important to note that a wide dynamic range is assured by the differential internal analog architecture and by the separate analog and digital voltage supplies and grounds.

A/D bandpass filter, A/D bandpass filter clocking, and A/D conversion timing

The A/D high-pass filter can be selected or bypassed via software control. The frequency response of this filter is presented in the following pages. This response results when the switched-capacitor filter clock frequency is 288 kHz and the A/D sample rate is 8 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz. The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 150 and 100 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 8 kHz.

The Internal Timing Configuration and AIC DX Data Word Format sections of this data sheet indicate the many options for attaining a 288-kHz bandpass switched-capacitor filter clock. These sections indicate that the RX Counter A can be programmed to give a 288-kHz bandpass switched-capacitor filter clock for several Master Clock input frequencies.

PRINCIPLES OF OPERATION (continued)

The A/D conversion rate is then attained by frequency-dividing the 288-kHz bandpass switched-capacitor filter clock with the RX Counter B. Thus, unwanted aliasing is prevented because the A/D conversion rate is an integral submultiple of the bandpass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D converter performance specifications

Fundamental performance specifications for the A/D converter circuitry are presented in the A/D converter operating characteristics section of this data sheet. The realization of the A/D converter circuitry with switched-capacitor techniques provides an inherent sample-and-hold.

analog output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A low-pass filter, D/A low-pass filter clocking, and D/A conversion timing

The frequency response of this filter is presented in the following pages. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz. Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 288 kHz. A continuous-time filter is provided on the output of the (sin x)/x filter to eliminate the periodic sample data signal information, which occurs at multiples of the 288-kHz switched-capacitor filter clock. The continuous time filter also greatly attenuates any switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 288-kHz switched-capacitor filter clock with TX Counter B. Thus, unwanted aliasing is prevented because the D/A conversion rate is an integral submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

asynchronous versus synchronous operation

If the transmit section of the AIC (low-pass filter and DAC) and receive section (bandpass filter and ADC) are operated asynchronously, the low-pass and bandpass filter clocks are independently generated from the Master Clock signal. Also, the D/A and A/D conversion rates are independently determined. If the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and bandpass filters. In synchronous operation, the A/D conversion timing is derived from, and is equal to, the D/A conversion timing. (See description of the WORD/$\overline{\text{BYTE}}$ pin in the Pin Functional Description Section.)

D/A converter performance specifications

Fundamental performance specifications for the D/A converter circuitry are presented in the D/A converter operating characteristics section of the data sheet. The D/A converter has a sample-and-hold that is realized with a switched-capacitor ladder.

system frequency response correction

(Sin x)/x correction for the D/A converter's zero-order sample-and-hold output can be provided by an on-board second-order (sin x)/x correction filter. This (sin x)/x correction filter can be inserted into or deleted from the signal path by digital signal processor control. When inserted, the (sin x)/x correction filter follows the switched-capacitor low-pass filter. When the TB register (see Internal Timing Configuration section) equals 36, the correction results of Figures 11 and 12 will be obtained.

PRINCIPLES OF OPERATION (continued)

(Sin x)/x correction can also be accomplished by deleting the on-board second-order correction filter and performing the (sin x)/x correction in digital signal processor software. The system frequency response can be corrected via DSP software to ±0.1 dB accuracy to a band-edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, which requires only seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of only 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (sin x)/x Correction Section for more details).

serial port

The serial port has four possible modes that are described in detail in the Functional Pin Description Section. These modes are briefly described below and in the Functional Description for Pin 13, WORD/$\overline{\text{BYTE}}$.

1. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS320C17.
2. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, and the TMS320C30.
3. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS320C17.
4. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, TMS320C30, or two SN74299 serial-to-parallel shift registers, which can then interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry.

operation of TLC32045 with internal voltage reference

The internal reference of the TLC32045 eliminates the need for an external voltage reference and provides overall circuit cost reduction. Thus, the internal reference eases the design task and provides complete control over the performance of the IC. The internal reference is brought out to a pin and is available to the designer. To keep the amount of noise on the reference signal to a minimum, an external capacitor may be connected between REF and ANLG GND.

operation of TLC32045 with external voltage reference

The REF pin may be driven from an external reference circuit if so desired. This external circuit must be capable of supplying 250 μA and must be adequately protected from noise such as crosstalk from the analog input

reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset fun · will initialize all AIC registers, including the control register. After a negative-going pulse on the · $\overline{\text{T}}$ pin, the AIC will be initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section).

PRINCIPLES OF OPERATION (Continued)

loopback

This feature allows the user to test the circuit remotely. In loopback, the OUT + and OUT − pins are internally connected to the IN + and IN − pins. Thus, the DAC bits (d15 to d2), which are transmitted to the DX pin, can be compared with the ADC bits (d15 to d2), which are received from the DR pin. An ideal comparison would be that the bits on the DR pin equal the bits on the DX pin. However, in practice there will be some difference in these bits due to the ADC and DAC output offsets.

The loopback feature is implemented with digital signal processor control by transmitting the appropriate serial port bit to the control register (see AIC Data Word Format section).

PIN NAME	PIN NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. Not internally connected to DGTL GND.
AUX IN +	24	I	Noninverting auxiliary analog input stage. This input can be switched into the bandpass filter and A/D converter path via software control. If the appropriate bit in the Control register is a 1, the auxiliary inputs will replace the IN + and IN − inputs. If the bit is a 0, the IN + and IN − inputs will be used (see the AIC DX Data Word Format section).
AUX IN −	23	I	Inverting auxiliary analog input (see the above AUX IN + pin description).
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
DR	5	O	This pin is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	This pin is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port to the AIC is synchronized with the SHIFT CLK signal.
$\overline{\text{EODR}}$	3	O	(See the WORD pin description and the Serial Port Timing Diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.

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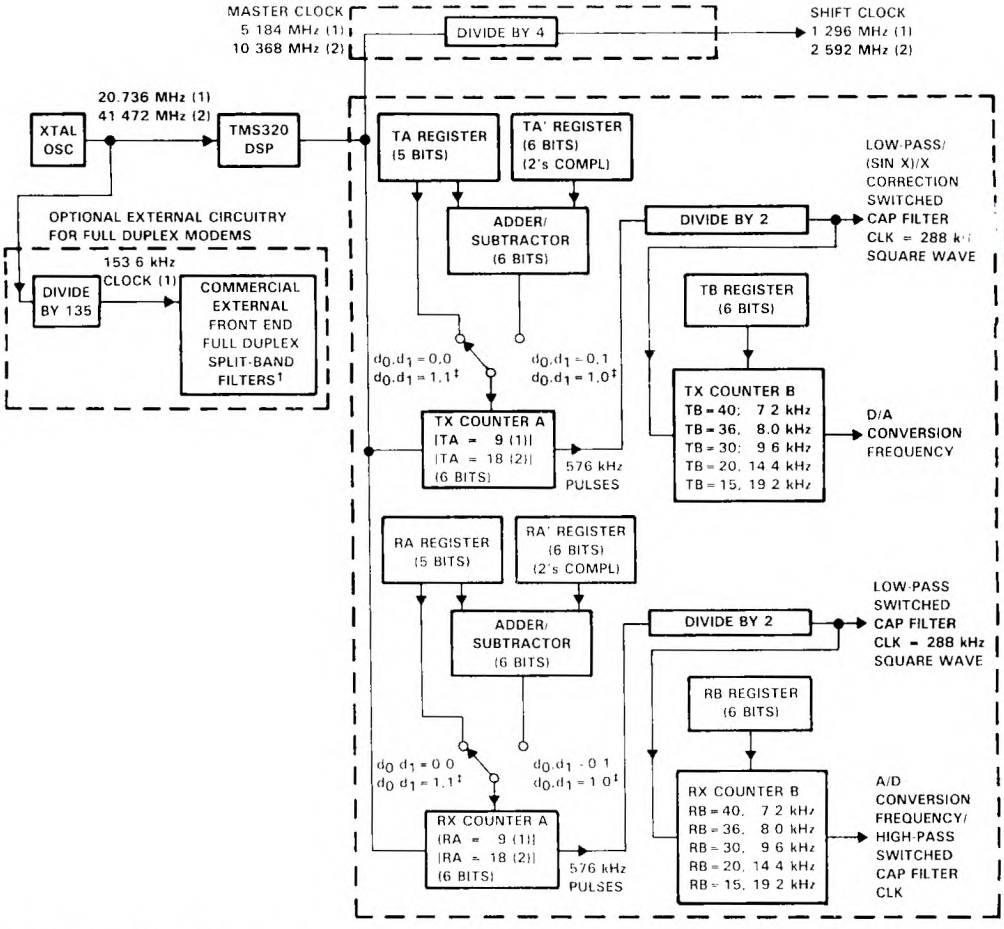
PIN NAME	PIN NO.	I/O	DESCRIPTION
$\overline{EODX}$	11	O	(See the WORD/$\overline{BYTE}$ pin description and the Serial Port Timing Diagram.) During the word-mode timing, this signal is a low-going pulse that occurs immediately after the 16 bits of D/A converter and control or register information have been transmitted from the TMS320 serial port to the AIC. This signal can be used to interrupt a microprocessor upon the completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or an external FIFO RAM, and to facilitate parallel data-bus communications between the AIC and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between the two bytes as to which is first and which is second.
$\overline{FSR}$	4	O	In the serial transmission modes, which are described in the WORD/$\overline{BYTE}$ pin description, the $\overline{FSR}$ pin is held low during bit transmission. When the $\overline{FSR}$ pin goes low, the TMS320 serial port will begin receiving bits from the AIC via the DR pin of the AIC. The most significant DR bit will be present on the DR pin before $\overline{FSR}$ goes low. (See Serial Port Timing and Internal Timing Configuration Diagrams.)
$\overline{FSX}$	14	O	When this pin goes low, the TMS320 serial port will begin transmitting bits to the AIC via the DX pin of the AIC. In all serial transmission modes, which are described in the WORD/$\overline{BYTE}$ pin description, the $\overline{FSX}$ pin is held low during bit transmission (see Serial Port Timing and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN−	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	The Master Clock signal is used to derive all the key logic signals of the AIC, such as the Shift Clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these key signals are synchronous submultiples of the Master Clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the A/D and D/A converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
OUT−	21	O	Inverting output of analog output power amplifier. Functionally identical with and complementary to OUT+.
REF	8	I/O	The internal voltage reference is brought out on this pin. An external voltage reference can also be applied to this pin.
$\overline{RESET}$	2	I	A reset function is provided to initialize the TA, TA', TB, RA, RA', RB, and control registers. This reset function initiates serial communications between the AIC and DSP. The reset function will initialize all AIC registers including the control register. After a negative-going pulse on the $\overline{RESET}$ pin, the AIC registers will be initialized to provide an 8-kHz data conversion rate for a 5.184-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', will be reset to 1. The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section). d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1 This initialization allows normal serial-port communication to occur between AIC and DSP.
SHIFT CLK	10	O	The Shift Clock signal is obtained by dividing the Master Clock signal frequency by four. This signal is used to clock the serial data transfers of the AIC, described in the WORD/$\overline{BYTE}$ pin description below (see the Serial Port Timing and Internal Timing Configuration diagram).
V_{DD}	7		Digital supply voltage, 5 V ±5%
$V_{CC}+$	20		Positive analog supply voltage, 5 V ±5%
$V_{CC}-$	19		Negative analog supply voltage −5 V ±5%

PIN NAME	NO.	I/O	DESCRIPTION
WORD/$\overline{\text{BYTE}}$	13	I	This pin, in conjunction with a bit in the CONTROL register, is used to establish one of four serial modes. These four serial modes are described below. *AIC transmit and receive sections are operated asynchronously.* The following description applies when the AIC is configured to have asynchronous transmit and receive sections. If the appropriate data bit in the Control register is a 0 (see the AIC DX Data Word Format), the transmit and receive sections will be asynchronous. L Serial port directly interfaces with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams). 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 8-bit byte is transmitted or one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought low. 4. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin emits a positive frame-sync pulse that is four Shift Clock cycles wide. 5. One 8-bit byte is transmitted or one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin is brought high. 7. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. H Serial port directly interfaces with the serial ports of the TMS32020, TMS320C25, and TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought low. 2. One 16-bit word is transmitted or one 16-bit word is received. 3. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pin is brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pin emits a low-going pulse. *AIC transmit and receive sections are operated synchronously.* If the appropriate data bit in the Control register is a 1, the transmit and receive sections will be configured to be synchronous. In this case, the bandpass switched-capacitor filter and the A/D conversion timing will be derived from the TX Counter A, TX Counter B, and TA, TA', and TB registers, rather than the RX Counter A, RX Counter B, and RA, RA', and RB registers. In this case, the AIC $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ timing will be identical during primary data communication; however, $\overline{\text{FSR}}$ will not be asserted during secondary data communication since there is no new A/D conversion result. The synchronous operation sequences are as follows (see Serial Port Timing diagrams). L Serial port directly interfaces with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 8-bit byte is transmitted and one 8-bit byte is received. 3. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought low. 4. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins emit positive frame-sync pulses that are four Shift Clock cycles wide. 5. One 8-bit byte is transmitted and one 8-bit byte is received. 6. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought high. 7. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. H Serial port directly interfaces with the serial ports of the TMS32020, TMS320C25, and TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows (see Serial Port Timing diagrams): 1. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought low. 2. One 16-bit word is transmitted and one 16-bit word is received. 3. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high. 4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pins emit low-going pulses. Since the transmit and receive sections of the AIC are now synchronous, the AIC serial port, with additional NOR and AND gates, will interface to two SN74299 serial-to-parallel shift registers. Interfacing the AIC to the SN74299 shift register allows the AIC to interface to an external FIFO RAM and facilitates parallel, data bus communications between the AIC and the digital signal processor. The operation sequence is the same as the above sequence (see Serial Port Timing diagrems).

INTERNAL TIMING CONFIGURATION



NOTE: Frequency 1, 20.736 MHz, is used to show how 153.6 kHz (for a commercially available modem split-band filter clock), popular speech and modem sampling signal frequencies, and an internal 288-kHz switched-capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched-capacitor filter stages. Frequency 2, 41.472 MHz, is used to show that the AIC can work with high-frequency signals, which are used by high-speed digital signal processors.

†Split-band filtering can alternatively be performed after the analog input function via software in the TMS320.

‡These control bits are described in the AIC DX Data Word Format section.

explanation of internal timing configuration

All of the internal timing of the AIC is derived from the high-frequency clock signal that drives the Master Clock input pin. The Shift Clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the Master Clock input signal frequency by four.

Low-pass:

$$\text{SCF Clock Frequency (D/A or A/D Path)} = \frac{\text{Master Clock Frequency}}{2 \times \text{Contents of Counter A}}$$

$$\text{Conversion Frequency} = \frac{\text{SCF Clock Frequency (D/A or A/D Path)}}{\text{Contents of Counter B}}$$

High-pass:

$$\text{SCF Clock Frequency (A/D Path)} = \text{A/D Conversion Frequency}$$

$$\text{Shift Clock Frequency} = \frac{\text{Master Clock Frequency}}{4}$$

TX Counter A and TX Counter B, which are driven by the Master Clock signal, determine the D/A conversion timing. Similarly, RX Counter A and RX Counter B determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path to meet its transfer function specifications, the frequency of its clock input must be 288 kHz. If the clock frequency is not 288 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 288 kHz. Thus, to obtain the specified filter response, the combination of Master Clock frequency and TX Counter A and RX Counter A values must yield a 288-kHz switched-capacitor clock signal. This 288-kHz clock signal can then be divided by the TX Counter B to establish the D/A conversion timing.

The transfer function of the bandpass switched-capacitor filter in the A/D path is a composite of its high-pass and low-pass section transfer functions. The high-frequency roll-off of the low-pass section will meet the bandpass filter transfer function specification when the low-pass section SCF is 288 kHz. Otherwise, the high-frequency roll-off will be frequency-scaled by the ratio of the high-pass section's SCF clock to 288 kHz. The low-frequency roll-off of the high-pass section will meet the bandpass filter transfer function specification when the A/D conversion rate is 8 kHz. Otherwise, the low-frequency roll-off of the high-pass section will be frequency-scaled by the ratio of the A/D conversion rate to 8 kHz.

TX Counter A and TX Counter B are reloaded every D/A conversion period, while RX Counter A and RX Counter B are reloaded every A/D conversion period. The TX Counter B and RX Counter B are loaded with the values in the TB and RB Registers, respectively. Via software control, the TX Counter A can be loaded with either the TA Register, the TA Register less the TA' Register, or the TA Register plus the TA' Register. By selecting the TA Register less the TA' Register option, the upcoming conversion timing will occur earlier by an amount of time that equals TA' times the signal period of the Master Clock. By selecting the TA Register plus the TA' Register option, the upcoming conversion timing will occur later by an amount of time that equals TA' times the signal period of the Master Clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. In this case, however, the RX Counter A can be programmed via software control with the RA Register, the RA Register less the RA' Register, or the RA Register plus the RA' Register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing. This feature can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous (see WORD/$\overline{\text{BYTE}}$ pin description), then both the low-pass and bandpass switched-capacitor filter clocks are derived from TX Counter A. Also, both the D/A and A/D conversion timing are derived from the TX Counter A and TX Counter B. When the transmit and receive sections are configured to be synchronous, the RX Counter A, RX Counter B, RA Register, RA' Register, and RB Registers are not used.

AIC DR or DX word bit pattern

A/D or D/A MSB, 1st bit sent — 1st bit sent of 2nd byte — A/D or D/A LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

AIC DX data word format section

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	COMMENTS
primary DX serial communication protocol																
← d15 (MSB) through d2 go to the D/A converter register →														0	0	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with TB and RB register values.
← d15 (MSB) through d2 go to the D/A converter register →														0	1	The TX and RX Counter A's are loaded with the TA + TA' and RA + RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 0, d0 = 1 will cause the next D/A and A/D conversion periods to be changed by the addition of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →														1	0	The TX and RX Counter A's are loaded with the TA − TA' and RA − RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: d1 = 1, d0 = 0 will cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to Table 1. AIC Responses to Improper Conditions.
← d15 (MSB) through d2 go to the D/A converter register →														1	1	The TX and RX Counter A's are loaded with the TA and RA register converter register values. The TX and RX Counter B's are loaded with the TB and RB register values. After a delay of four Shift Clock cycles, a secondary transmission will immediately follow to program the AIC to operate in the desired configuration.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (Primary Communications) to the AIC will initiate Secondary Communications upon completion of the Primary Communications.

Upon completion of the Primary Communication, $\overline{\text{FSX}}$ will remain high for four SHIFT CLOCK cycles and will then go low and initiate the Secondary Communication. The timing specifications for the Primary and Secondary Communications are identical. In this manner, the Secondary Communication, if initiated, is interleaved between successive Primary Communications. This interleaving prevents the Secondary Communication from interfering with the Primary Communications and DAC timing, thus preventing the AIC from skipping a DAC output. It is important to note that in the synchronous mode, $\overline{\text{FSR}}$ will not be asserted during Secondary Communications

secondary DX serial communication protocol

x x | ← to TA register → | x x | ← to RA register → | 0 0	d13 and d6 are MSBs (unsigned binary)
x | ← to TA′ register → | x | ← to RA′ register → | 0 1	d14 and d7 are 2's complement sign bits
x | ← to TB register → | x | ← to RB register → | 1 0	d14 and d7 are MSBs (unsigned binary)
x x x x x x d9 x d7 d6 d5 d4 d3 d2 1 1 CONTROL REGISTER	d2 = 0/1 deletes/inserts the A/D highpass filter d3 = 0/1 disables/enables the loopback function d4 = 0/1 disables/enables the AUX IN + and AUX IN − pins d5 = 0/1 asynchronous/synchronous transmit and receive sections d6 = 0/1 gain control bits (see Gain Control Section) d7 = 0/1 gain control bits (see Gain Control Section) d9 = 0/1 delete/insert on-board second-order (sin x)/x correction filter

reset function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function will initialize all AIC registers, ding the control register. After power has been applied to the AIC, a negative-going pulse on the R· · pin will initialize the AIC registers to provide an 8-kHz A/D and D/A conversion rate for a 5.184 MHz master clock input signal. The AIC, excepting the CONTROL register, will be initialized as follows (see AIC DX Data Word Format section):

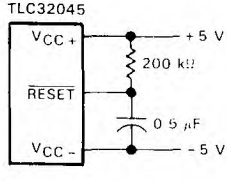
REGISTER	INITIALIZED REGISTER VALUE (HEX)
TA	9
TA′	1
TB	24
RA	9
RA′	1
RB	24

The CONTROL register bits will be reset as follows (see AIC DX Data Word Format section):

d9 = 1, d7 = 1, d6 = 1, d5 = 1, d4 = 0, d3 = 0, d2 = 1

This initialization allows normal serial port communications to occur between AIC and DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA′, and TB register need to be programmed, since both transmit and receive timing are synchronously derived from these registers (see the Pin Descriptions and AIC DX Word Format sections).

The circuit shown below will provide a reset on power-up when power is applied in the sequence given under Power-Up Sequence. The circuit depends on the power supplies' reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.



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power-up sequence

To ensure proper operation of the AIC, and as a safeguard against latch-up, it is recommmended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND (see Figure 21). In the absence of such diodes, power should be applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input *signal* should be applied until after power-up.

AIC responses to improper conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 1 below.

AIC register constraints

The following constraints are placed on the contents of the AIC registers:

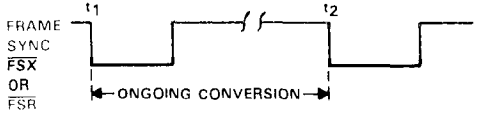
1. TA register must be > 1.
2. TA' register can be either positive, negative, or zero.
3. RA register must be > 1.
4. RA' register can be either positive, negative, or zero.
5. (TA register ± TA' register) must be > 1.
6. (RA register ± RA' register) must be > 1.
7. TB register must be > 1.

TABLE 1. AIC RESPONSES TO IMPROPER CONDITIONS

IMPROPER CONDITION	AIC RESPONSE
TA register + TA' register = 0 or 1 TA register − TA' register = 0 or 1	Reprogram TX Counter A with TA register value
TA register + TA' register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into the TX Counter A, i.e., TA register + TA' register + 40 HEX is loaded into TX Counter A
RA register + RA' register = 0 or 1 RA register − RA' register = 0 or 1	Reprogram RX Counter A with RA register value
RA register + RA' register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX Counter A, i.e., RA register + RA' register + 40 HEX is loaded into RX Counter A
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down
TB register = 0 or 1	Reprogram TB register with 24 HEX
RB register = 0 or 1	Reprogram RB register with 24 HEX
AIC and DSP cannot communicate	Hold last DAC output

improper operation due to conversion times being too close together

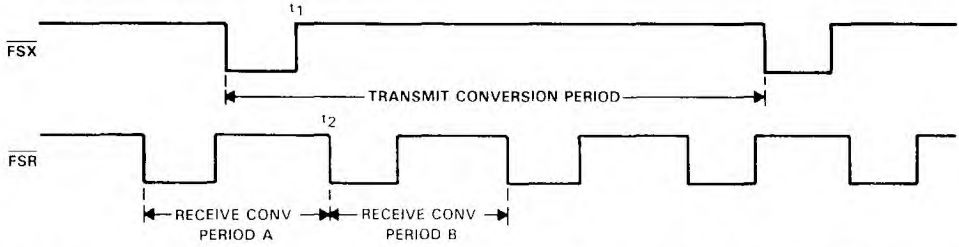
If the difference between two successive D/A conversion frame syncs is less that 1/19.2 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A' register or A − A' register result is too small. When incrementally adjusting the conversion period via the A + A' register options, the designer should be very careful not to violate this requirement (see diagram below).



$t_2 - t_1 > 1/19.2$ kHz

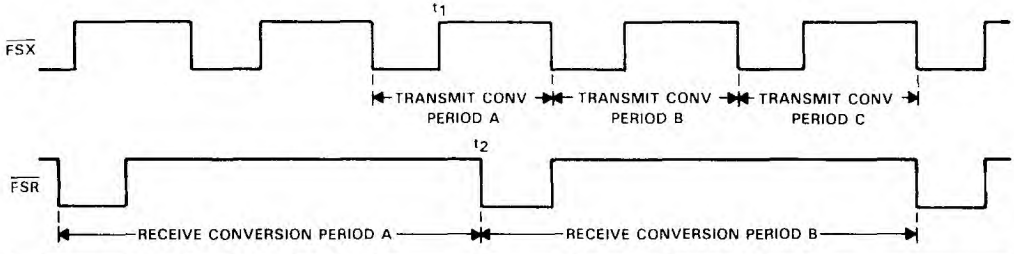
asynchronous operation — more than one receive frame sync occurring between two transmit frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing conversion period is then adjusted. However, either Receive Conversion Period A or B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. Therefore, if there is sufficient time between t1 and t2, the receive conversion period adjustment will be performed during Receive Conversion Period A. Otherwise, the adjustment will be performed during Receive Conversion Period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent $\overline{FSX}$ frame (see figure below).



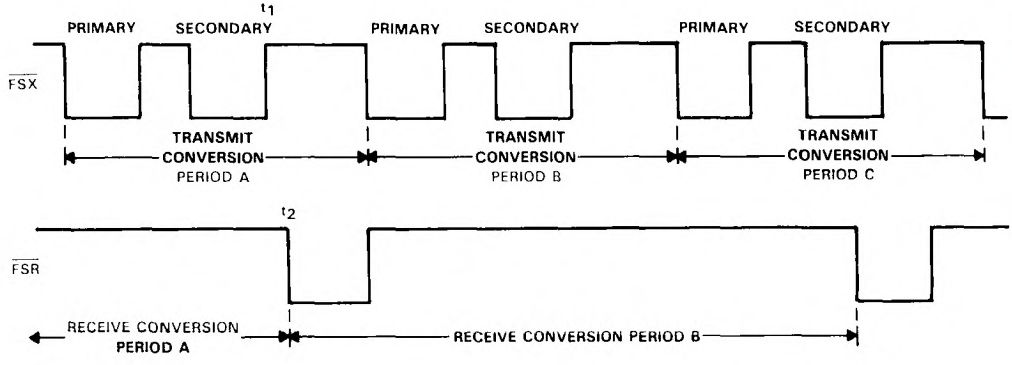
asynchronous operation — more than one transmit frame sync occurring between two receive frame syncs

When incrementally adjusting the conversion period via the A + A′ or A − A′ register options, a specific protocol is followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during a $\overline{FSX}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment in the diagram as shown in the figure below. If the adjustment command is issued during Transmit Conversion Period A, Receive Conversion Period A will be adjusted if there is sufficient time between t1 and t2. Or, if there is not sufficient time between t1 and t2, Receive Conversion Period B will be adjusted. Or, the receive portion of an adjustment command may be ignored if the adjustment command is sent during a receive conversion period, which is already being or will be adjusted due to a prior adjustment command. For example, if adjustment commands are issued during Transmit Conversion Periods A, B, and C, the first two commands may cause Receive Conversion Periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during Receive Conversion Period B, which already will be adjusted via the Transmit Conversion Period B adjustment command.



asynchronous operation — more than one set of primary and secondary DX serial communication occurring between two receive frame sync (see AIC DX Data Word Format section)

The TA, TA′, TB, and control register information that is transmitted in the secondary communications is always accepted and is applied during the ongoing transmit conversion period. If there is sufficient time between t1 and t2, the TA, RA′, and RB register information, which is sent during Transmit Conversion Period A, will be applied to Receive Conversion Period A. Otherwise, this information will be applied during Receive Conversion Period B. If RA, RA′, and RB register information has already been received and is being applied during an ongoing conversion period, any subsequent RA, RA′, or RB information that is received during this receive conversion period will be disregarded (see diagram below).



test modes†

The following paragraph provides information that allows the TLC32045 to be operated in special test modes. These test modes are used by Texas Instruments to facilitate testing of the device during manufacturing. They are not intended to be used in real applications, however, they allow the filters in the A/D and D/A paths to be used without using the A/D and D/A converters.

In normal operation, the nonusable (NU) pins are left unconnected. These NU pins are used by the factory to speed up testing of the TLC32045 Analog Interface Circuit (AIC). When the device is used in normal (non-test mode) operation, the NU pin (pin 1) has an internal pull-down to −5 V. Externally connecting 0 V or 5 V to pin 1 puts the device in test-mode operation. Selecting one of the possible test or NU modes is accomplished by placing a particular voltage on certain pins. A description of these modes is provided in Table 2 and Figures 1 and 2.

TABLE 2. LIST OF TEST MODES

TEST PINS	D/A PATH TEST (PIN 1 to 5 V) TEST FUNCTION	A/D PATH TEST (PIN 1 to 0) TEST FUNCTION
5	The low-pass switched-capacitor filter clock is brought out to pin 5. This clock signal is normally internal.	The bandpass switched-capacitor filter clock is brought out to pin 5. This clock signal is normally internal.
11	No change from normal operation. The $\overline{EODX}$ signal is brought out to pin 11.	The pulse that initiates the A/D conversion is brought out here. This signal is normally internal.
3	The pulse that initiates the D/A conversion is brought out here.	No change from normal operation. The EODR signal is brought out.
27 and 28	There are no test output signals provided on these pins.	The outputs of the A/D path low-pass or bandpass filter (depending upon control bit d2 − see AIC DX Data Word Format section) are brought out to these pins. If the high-pass section is inserted, the output will have a (sinx)/x droop. The slope of the droop will be determined by the ADC sampling frequency, which is the high-pass section clock frequency (see diagram of bandpass or low-pass filter test for receive section). These outputs will drive small (30-pF) loads.
	D/A PATH LOW-PASS FILTER TEST; PIN 13 (WORD/BYTE) to −5 V	
	TEST FUNCTION	
15 and 16	The inputs of the D/A path low-pass filter are brought out to pins 15 and 16. The D/A input to this filter is removed. If the (sin x)/x correction filter is inserted, the OUT+ and OUT− signals will have a flat response (see Figure 2). The common-mode range of these inputs must not exceed ±0.5 V.	

† In the test mode, the AIC responds to the setting of Pin 13 to −5 V, as if Pin 13 were set to 0 V. Thus, the byte mode is selected for communicating between DSP and AIC. Either of the path tests (D/A or A/D) can be performed simultaneously with the D/A low-pass filter test. In this situation, Pin 13 must be connected to −5 V, which initiates byte-mode communications.

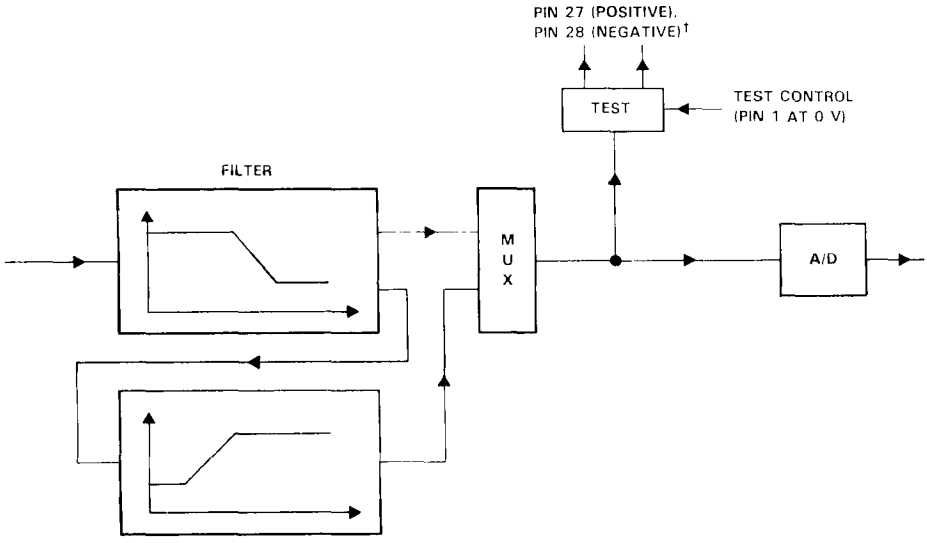


FIGURE 1. BANDPASS OR LOW-PASS FILTER TEST FOR RECEIVER SECTION

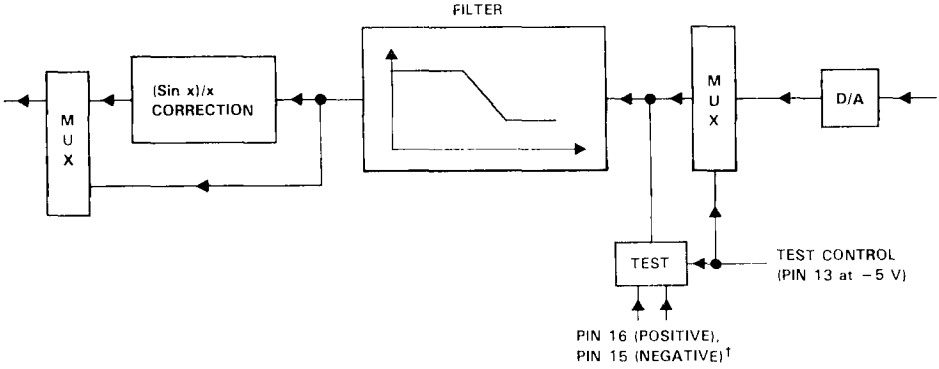


FIGURE 2. LOW-PASS FILTER TEST FOR TRANSMIT SECTION

†All analog signal paths have differential architecture and hence have positive and negative components.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . −0.3 V to 15 V
Supply voltage, V_{DD} . . . . . −0.3 V to 15 V
Output voltage, V_O . . . . . −0.3 V to 15 V
Input voltage, V_I . . . . . −0.3 V to 15 V
Digital ground voltage . . . . . −0.3 V to 15 V
Operating free-air temperature range: TLC32045I . . . . . −40°C to 85°C
TLC32045C . . . . . 0°C to 70°C
Storage temperature range . . . . . −40°C to 125°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: Voltage values for maximum ratings are with respect to VCC−.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}+0.3	V
Low-level input voltage, V_{IL} (see Note 3)		−0.3		0.8	V
Load resistance at OUT+ and/or OUT−, R_L		300			Ω
Load capacitance at OUT+ and/or OUT−, C_L				100	pF
MSTR CLK frequency (see Note 4)		0.075	5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				19.2	kHz
Conversion rate		1		20	kHz
Operating free-air temperature, T_A	TLC··5I	−40		85	°C
	TLC··5C	0		70	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-}, are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.
4. The bandpass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 8 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF clock is shifted from 8 kHz, the high-pass roll-off frequency will shift by the ratio of the high-pass SCF clock to 8 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency will shift by the ratio of the SCF clock to 288 kHz.
5. This range applies when (IN+ − IN−) or (AUX IN+ − AUX IN−) equals ±6 V.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC32045I				45	mA
		TLC32045C				40	
I_{CC-}	Supply current from V_{CC-}	TLC32045I				−45	mA
		TLC32045C				−40	
I_{DD}	Supply current from V_{DD}		$f_{MSTR\ CLK}$ = 5.184 MHz			7	mA
V_{ref}	Internal reference output voltage			2.9		3.4	V
αV_{ref}	Temperature coefficient of internal reference voltage				250		ppm/°C
r_o	Output resistance at REF				100		kΩ

receive amplifier input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters in)			10	75	mV
CMRR	Common-mode rejection ratio at IN+, IN−, or AUX IN+, AUX IN−	See Note 6		55		dB
r_I	Input resistance at IN+, IN− or AUX IN+, AUX IN−, REF			100		kΩ

transmit filter output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT− (single-ended relative to ANLG GND)			15	80	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT− (single-ended)	$R_L \geq 300\ \Omega$, Offset voltage = 0	±3			V
V_{OM}	Maximum peak output voltage swing between OUT+ and OUT− (differential output)	$R_L \geq 600\ \Omega$	±6			V

†All typical values are at T_A = 25°C.

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with an 8-kHz conversion rate.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

system distortion specifications, SCF clock frequency = 288 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	V_{in} = −0.1 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	differential		55	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended	V_{in} = −0.1 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	differential		55	65		
Attenuation of second harmonic of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 7		70		dB
	differential		55	70		
Attenuation of third and higher harmonics of D/A input signal	single-ended	V_{in} = −0 dB to −24 dB referred to V_{ref}, See Note 7		65		dB
	differential		55	65		

A/D channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	A_V = 1‡		A_V = 2‡		A_V = 4‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	55		>55§		>55§		dB
	V_{in} = −12 dB to −6 dB	55		55		>55§		
	V_{in} = −18 dB to −12 dB	53		55		55		
	V_{in} = −24 dB to −18 dB	47		53		55		
	V_{in} = −30 dB to −24 dB	41		47		53		
	V_{in} = −36 dB to −30 dB	35		41		47		
	V_{in} = −42 dB to −36 dB	29		35		41		
	V_{in} = −48 dB to −42 dB	23		29		35		
	V_{in} = −54 dB to −48 dB	17		23		29		

D/A channel signal-to-distortion ratio

PARAMETER	TEST CONDITIONS (see Note 7)	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_{in} = −6 dB to −0.1 dB	55		dB
	V_{in} = −12 dB to −6 dB	55		
	V_{in} = −18 dB to −12 dB	53		
	V_{in} = −24 dB to −18 dB	47		
	V_{in} = −30 dB to −24 dB	41		
	V_{in} = −36 dB to −30 dB	35		
	V_{in} = −42 dB to −36 dB	29		
	V_{in} = −48 dB to −42 dB	23		
	V_{in} = −54 dB to −48 dB	17		

† All typical values are at T_A = 25°C.
‡ A_V is the programmable gain of the input amplifier
§ A value >55 is over range and signal clipping occurs
NOTE 7: The test condition is a 1-kHz input signal with an 8-kHz conversion rate (0 dB relative to V_{ref}). The load impedance for the DAC is 600 Ω.

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electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (unless otherwise noted)

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Absolute transmit gain tracking error while transmitting into 600 Ω	−42 dB to 0 dB signal range, See Note 8		±0.05	±0.15	dB
Absolute receive gain tracking error	−42 dB to 0 dB signal range, See Note 8		±0.05	±0.15	dB

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single-ended)				75		dB

†All typical values are at T_A = 25°C.

NOTE: 8. Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

delay distortion

bandpass filter transfer function, SCF f_{clock} = 288 kHz IN+ − IN− is a ±3 V sinewave† (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Gain relative to gain at 1 kHz (except passband ripple specification)	Input signal reference is 0 dB (see Note 9)	f ≤ 50 Hz	K1 × 0 dB	−33	−29	−25	dB
		f = 100 Hz	K1 × − 0.26 dB	−4	−2	−1	
		f = 150 Hz to 3100 Hz	K1 × 0 dB	−0.25	0	0.25	
		f = 3100 Hz to 3300 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 3300 Hz to 3650 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB	−5	−3	−1	
		f = 4000 Hz	K1 × 2.7 dB	−20	−17	−16	
		f ≥ 4400 Hz	K1 × 3.2 dB			−40	
		f ≥ 5000 Hz	K1 × 0 dB			−65	

low-pass filter transfer function (see curves), SCF f_{clock} = 288 kHz (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP§	MAX	UNIT
Gain relative to gain at 1 kHz (except passband ripple specification)	Input signal reference is 0 dB (see Note 9)	f = 0 Hz to 3100 Hz	K1 × 0 dB	−0.25	0	0.25	dB
		f = 3 Hz to Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 3 Hz to Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 3800 Hz	K1 × 2.3 dB	−5	−3	−1	
		f = 4000 Hz	K1 × 2.7 dB	−20	−17	−16	
		f ≥ 4400 Hz	K1 × 3.2 dB			−40	
		f ≥ 5000 Hz	K1 × 0 dB			−65	

serial port

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −300 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	μA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† See filter curves in typical characteristics.

‡ The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 • [(SCF frequency − 288 kHz)/ 288 kHz]. For errors greater than 0.25%, see Note 10.

§ All typical values are at T_A = 25°C.

NOTES: 9. The filter gain outside of the passband is measured with respect to the gain at 1 kHz. The filter gain within the passband is measured with respect to the average gain within the passband. The passbands are 150 to 3600 Hz and 0 to 3600 Hz for the bandpass and low-pass filters respectively.

10. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

noise (measurement includes low-pass and bandpass switched-capacitor filters)

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
Transmit noise	with (sin x)/x correction	DX input = 00000000000000, constant input code		600	μV rms
	without (sin x)/x correction			450	μV rms
			24		dBrnc0
Receive noise (see Note 11)		Inputs grounded, gain = 1		530	μV rms
			24		dBrnc0

timing requirements

serial port recommended input signals

PARAMETER		MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	$\overline{RESET}$ pulse duration (see Note 12)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/4$		ns

† All typical values are at T_A = 25°C.

NOTES: 11. The noise is computed by statistically evaluating the digital output of the A/D converter.

12. $\overline{RESET}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

operating characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (continued)

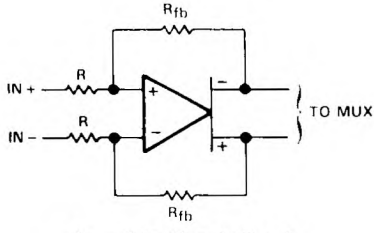
serial port — AIC output signals

PARAMETER		MIN	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		50	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		50	ns
	Shift clock (SCLK) duty cycle	45	55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}$↓		90	ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{FSR}/\overline{FSX}$↑		90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑		90	ns
$t_{dw(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in word mode		90	ns
$t_{dw(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in word mode		90	ns
$t_{f(EODX)}$	$\overline{EODX}$ fall time		15	ns
$t_{f(EODR)}$	$\overline{EODR}$ fall time		15	ns
$t_{db(CH-EL)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↓ in byte mode		100	ns
$t_{db(CH-EH)}$	Delay from SCLK↑ to $\overline{EODX}/\overline{EODR}$↑ in byte mode		100	ns

TABLE 2. GAIN CONTROL TABLE
(ANALOG INPUT SIGNAL REQUIRED FOR FULL-SCALE A/D CONVERSION)

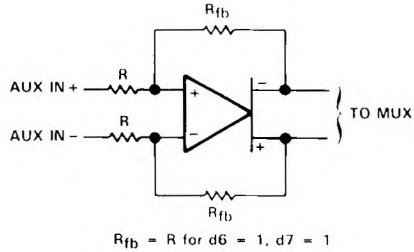
INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT†	A/D CONVERSION RESULT
	d6	d7		
Differential configuration	1	1	±6 V	full-scale
Analog input = IN+ − IN−	0	0		
= AUX IN+ − AUX IN−	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale
Single-ended configuration	1	1	±3 V	half-scale
Analog input = IN+ − ANLG GND	0	0		
= AUX IN+ − ANLG GND	1	0	±3 V	full-scale
	0	1	±1.5 V	full-scale

† In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0 d7 = 1

FIGURE 3. IN+ AND IN− GAIN CONTROL CIRCUITRY



R_{fb} = R for d6 = 1, d7 = 1
d6 = 0, d7 = 0
R_{fb} = 2R for d6 = 1, d7 = 0
R_{fb} = 4R for d6 = 0 d7 = 1

FIGURE 4. AUX IN+ AND AUX IN− GAIN CONTROL CIRCUITRY

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(sin x)/x correction section

If the designer does not wish to use the on-board second-order (sin x)/x correction filter, correction can be accomplished in digital signal processor (DSP) software. (Sin x)/x correction can be accomplished easily and efficiently in digital signal processor (DSP) software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results, which are shown below, are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires only seven instruction cycles per sample on the TMS320 DSPs. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction will add a slight amount of group delay at the upper edge of the 300–3000-Hz band.

(sin x)/x roll-off for a zero-order hold function

The (sin x)/x roll-off for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in the table below.

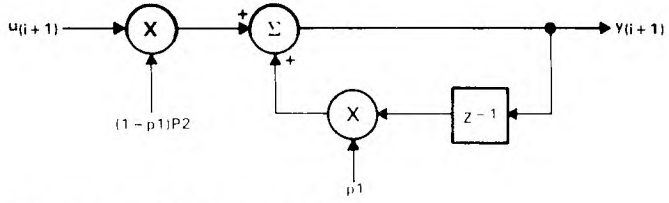
TABLE 3. (sin x)/x ROLL-OFF

f_s (Hz)	$20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ (f = 3000 Hz) (dB)
7200	- 2 64
8000	- 2.11
9600	- 1 44
14400	0 63
19200	- 0 35

Note that the actual AIC (sin x)/x roll-off will be slightly less than the above figures, because the AIC has less than a 100% duty cycle hold interval.

correction filter

To compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter shown below, is recommended.



The difference equation for this correction filter is:

$$y_{i+1} = p2(1-p1)\,(u_{i+1}) + p1\,y_i$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{p2^2\,(1-p1)^2}{1 - 2p1\cos(2\pi f/f_S) + p1^2}$$

correction results

Table 4 below shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates.

TABLE 4

f (Hz)	ERROR (dB) f_s = 8000 Hz p1 = −0.14813 p2 = 0 9888	ERROR (dB) f_s = 9600 Hz p1 = −0.1307 p2 = 0.9951
300	- 0 099	- 0 043
600	− 0 089	− 0 043
900	- 0.054	0
1200	- 0 002	0
1500	0 041	0
1800	0 079	0 043
2100	0 100	0.043
2400	0 091	0 043
2700	- 0 043	0
3000	-- 0 102	- 0 043

TMS320 software requirements

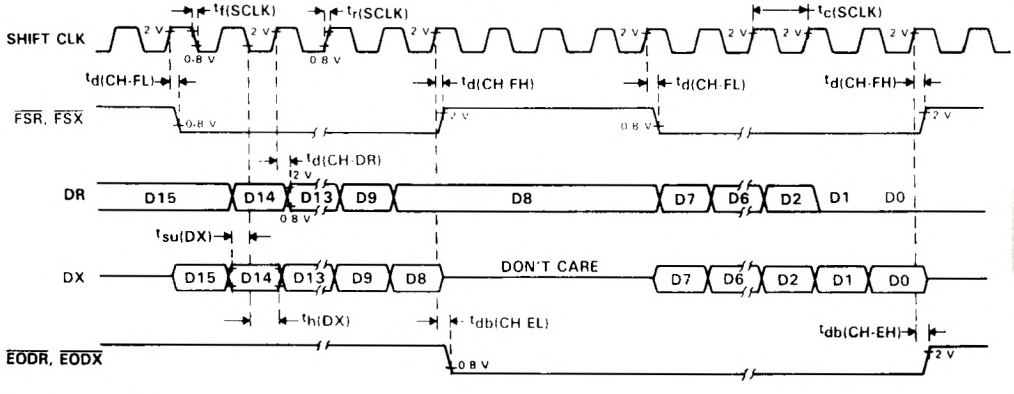
The digital correction filter equation can be written in state variable form as follows:

$$Y = k1Y + k2U$$

where k1 equals p1 (from the preceding page), k2 equals (1 − p1)p2 (from the preceding page), Y is the filter state, and U is the next I/O sample. The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) will yield the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

byte-mode timing



word-mode timing

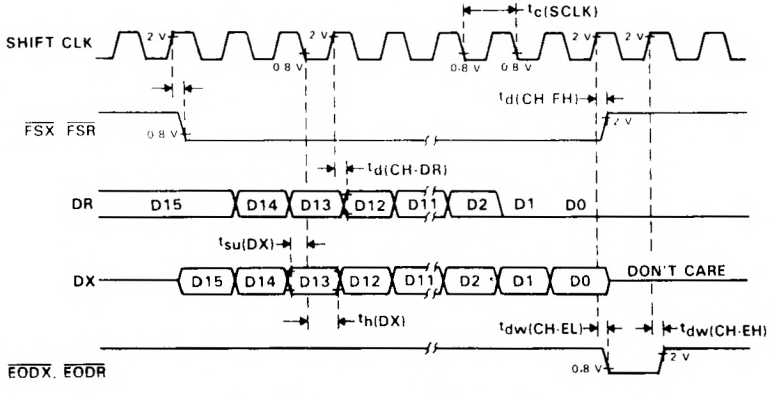


FIGURE 5. SERIAL PORT TIMING

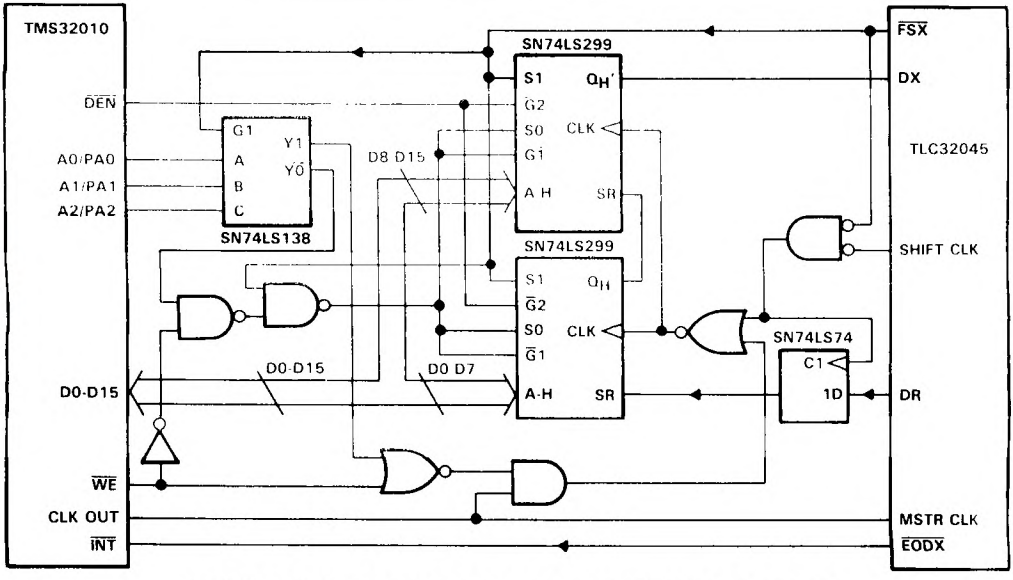
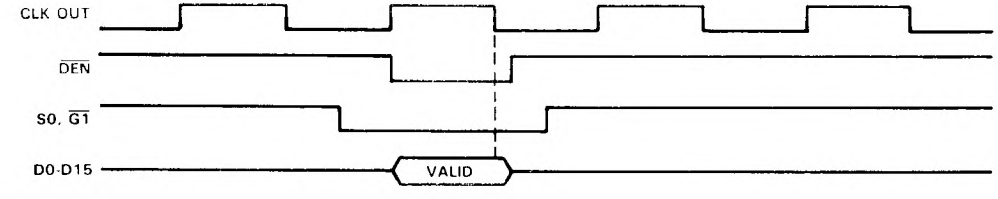


FIGURE 6. TMS32010/TMS320C15-TLC32045 INTERFACE CIRCUIT

in instruction timing



out instruction timing

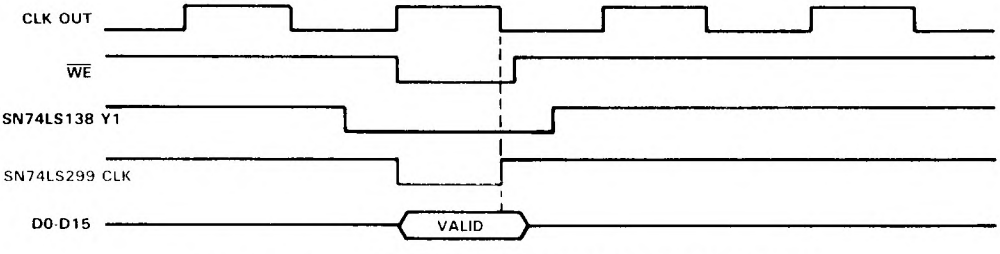


FIGURE 7. TMS32010/TMS320C15-TLC32045 INTERFACE TIMING

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

AIC TRANSMIT AND RECEIVE LOW-PASS FILTER

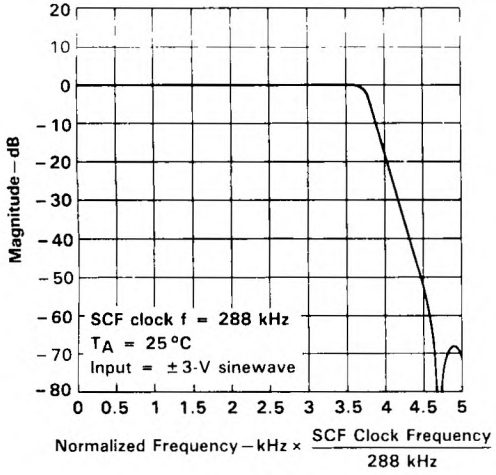

FIGURE 8

AIC TRANSMIT AND RECEIVE LOW-PASS FILTER

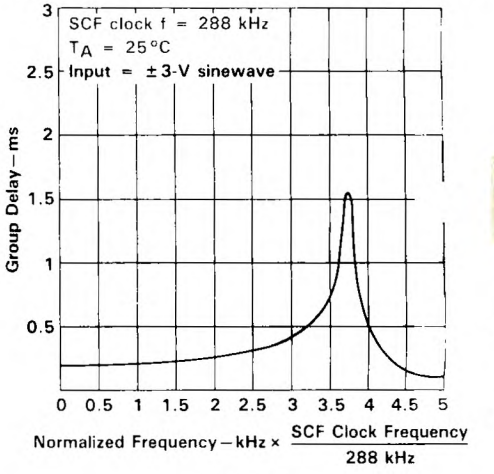

FIGURE 9

AIC RECEIVE-CHANNEL BANDPASS FILTER

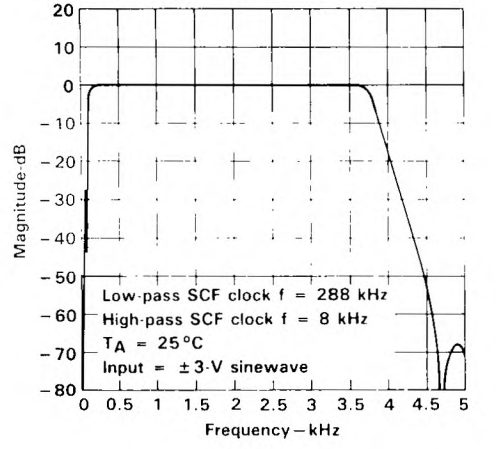

FIGURE 10

AIC RECEIVE-CHANNEL HIGH-PASS FILTER

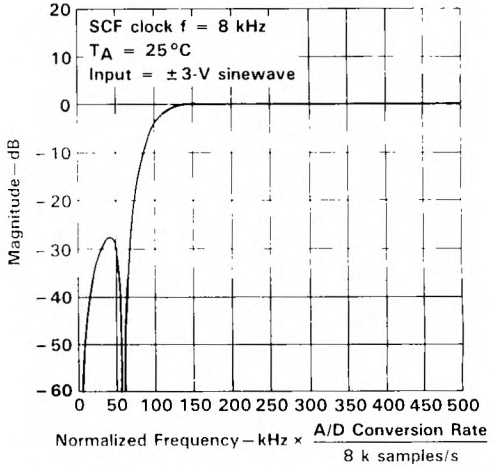

FIGURE 11

TYPICAL CHARACTERISTICS

AIC RECEIVE CHANNEL BANDPASS FILTER

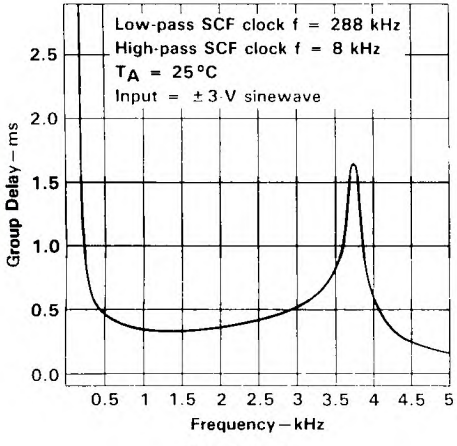

FIGURE 12

AIC (SIN X)/X CORRECTION FILTER

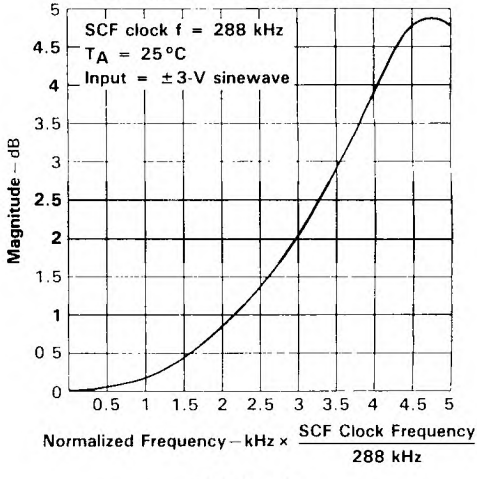

FIGURE 13

(SIN X)/X CORRECTION FILTER

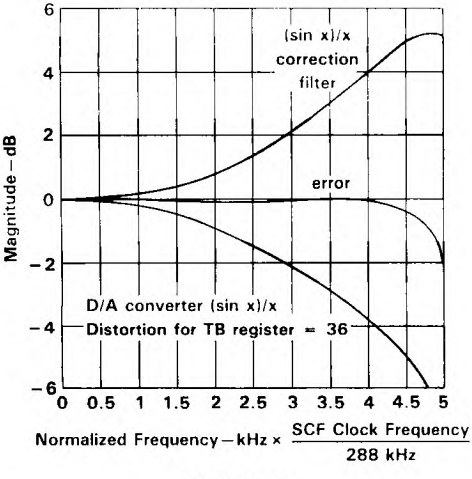

FIGURE 14

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

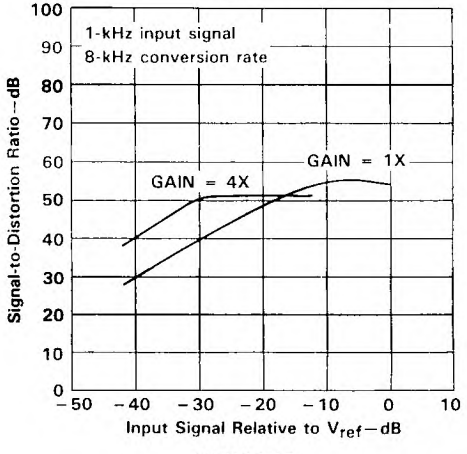

FIGURE 15

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN AT 0 dB INPUT SIGNAL)

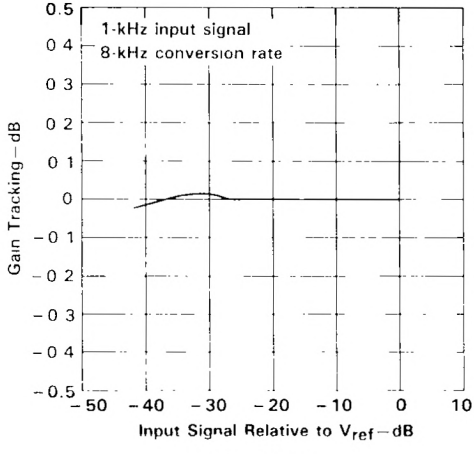


FIGURE 16

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL LEVEL

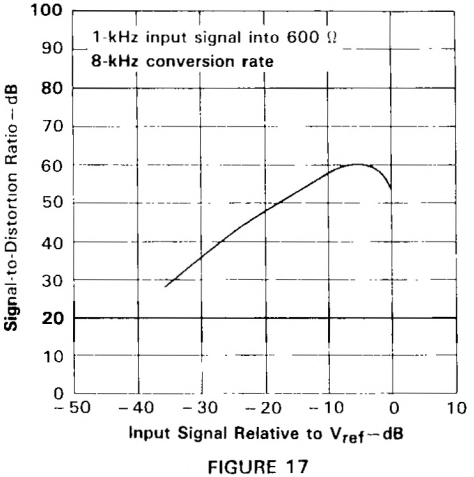


FIGURE 17

TYPICAL CHARACTERISTICS

D/A GAIN TRACKING
(GAIN RELATIVE TO GAIN
AT 0 dB INPUT SIGNAL LEVEL)

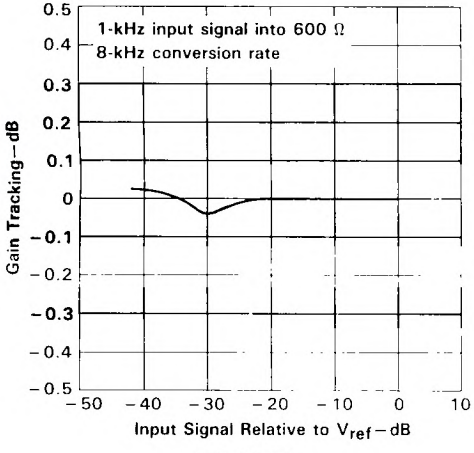


FIGURE 18

A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

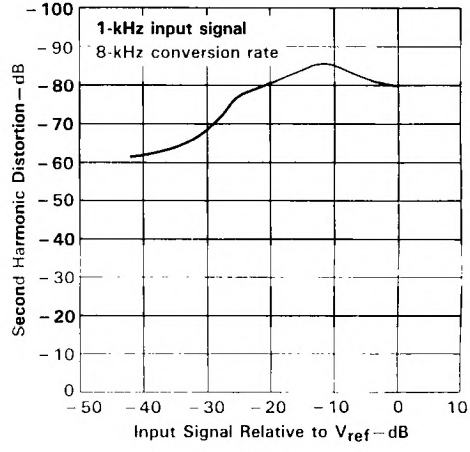


FIGURE 19

D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

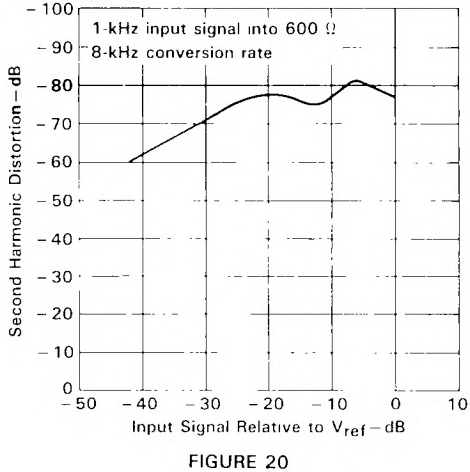


FIGURE 20

TYPICAL CHARACTERISTICS

A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

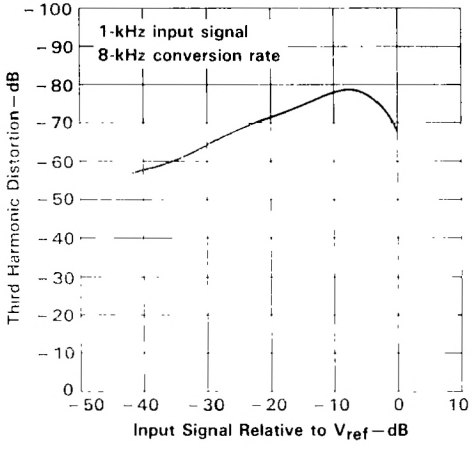


FIGURE 21

D A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

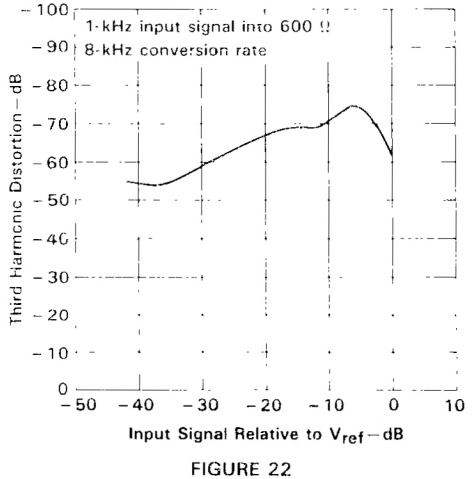
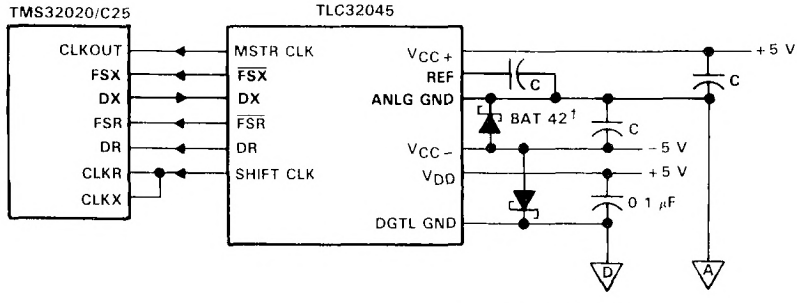


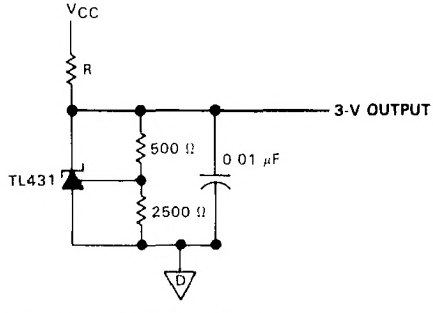
FIGURE 22

TYPICAL APPLICATION INFORMATION



C = 0.2 μF, CERAMIC

FIGURE 23. AIC INTERFACE TO THE TMS32020/C25 SHOWING DECOUPLING CAPACITORS AND SCHOTTKY DIODE†



FOR: V_{CC} = 12 V, R = 7200 Ω
V_{CC} = 10 V, R = 5600 Ω
V_{CC} = 5 V, R = 1600 Ω

FIGURE 24. EXTERNAL REFERENCE CIRCUIT FOR TLC32045

†Thomson Semiconductors